SET VOLTAGE DISTRIBUTION STABILIZED BY CONSTRUCTING AN OXYGEN RESERVOIR IN RESISTIVE RANDOM ACCESS MEMORY

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Key Words: RRAM, interface-type, oxygen accumulation, instability mechanism

In this letter, the instability mechanism of RRAM was investigated, and a technique was developed to stabilize the distribution of high resistance state (HRS) and better concentrate the SET voltage. In previous research, we found that an interface-type switching characteristic was observed on the I-V curve beneath the filament-type switching behavior, owing to the oxygen accumulation effect. In this letter, this interface-type switching characteristic is used to fit the natural distribution of HRS for an analysis of the instability mechanism. According to the results, the reason for the HRS distribution is the accumulation of extra oxygen ions which are left over from a lower degree of oxygen and oxygen vacancy recombination during the reset process. We propose a solution which creates an extra oxygen reservoir by changing the surface topography of the electrode to store the surplus oxygen ions from the reset process, eliminating the accumulation effect, and indeed improving stability.

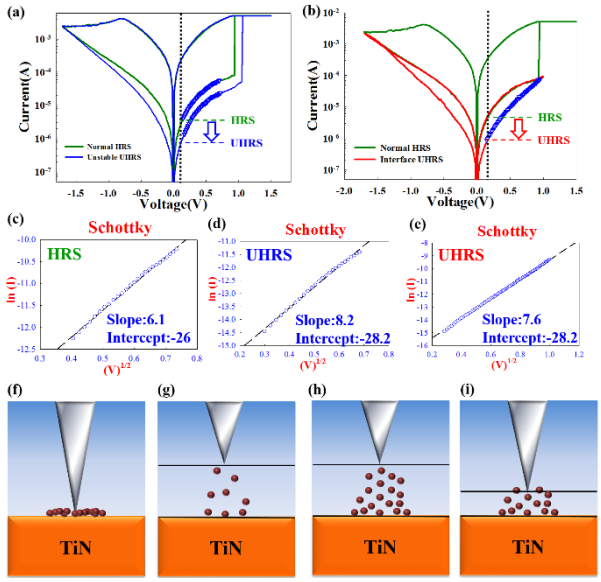

Figure 1 – (a) The HRS and the UHRS sweep cycle in normal RRAM. (b) UHRS achieved by interface-type switching. Fitting result of (c) HRS, (d) unstable UHRS, and (e) interface UHRS. The conduction model of (f) LRS, (g) HRS, (h) interface UHRS, and (i) unstable UHRS.

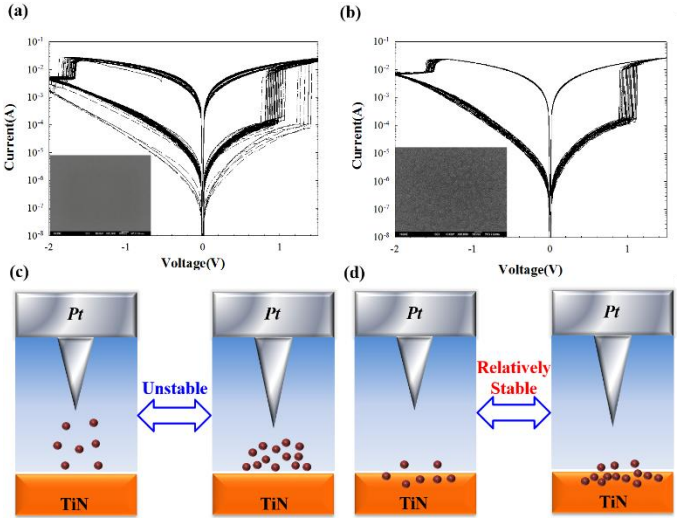

Figure 2 – The distribution of the I-V characteristic (a) before and (b) after CF4 plasma treatment and the SEM image on bottom left. The conduction model (c) before and (d) after CF4 plasma treatment.

INVESTIGATION OF DEGRADATION CAUSED BY CHARGE TRAPPING AT ETCHING-STOP LAYER UNDER AC GATE-BIAS STRESS FOR InGaZnO THIN FILM TRANSISTORS

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Key Words: Indium-Galium-Zinc-Oxide, Positive Bias Stress, Alternative current, Etching-stop layer

A great amount of literatures has been focusing on bias-induced instability issues including threshold voltage shift (ΔVt) and subthreshold swing (S.S) degradations [1]. However, in practical TFT operation circuits, very limited knowledge could be applied since operation modes are mostly applied with alternative current (AC). Based on these backgrounds, in this work, Indium-Gallium-Zinc-Oxide Thin Film Transistors (IGZO TFTs) are applied with AC PBS degradations. Compared with previous work, this work observed a structure dependent degradation. An etch-stop structure IGZO TFT observed a serious threshold voltage shift after AC stress but shown great stability after direct current (DC) stress. The device structure and transfer characteristic curves are demonstrated in Figure 1(a) and (b) respectively. From results of DC PBS/NBS, a favorable stability indicating a great quality of gate insulator. Therefore, the positive threshold voltage shift is believed to be origin from electron trapping at the etching stop layer (ESL), since ESL possesses a relatively poor quality compared to the gate insulator. The charge trapping at etching stop layer could be confirmed by results of asymmetric source/drain metal under AC stress, illustrated in Figure 1(c).

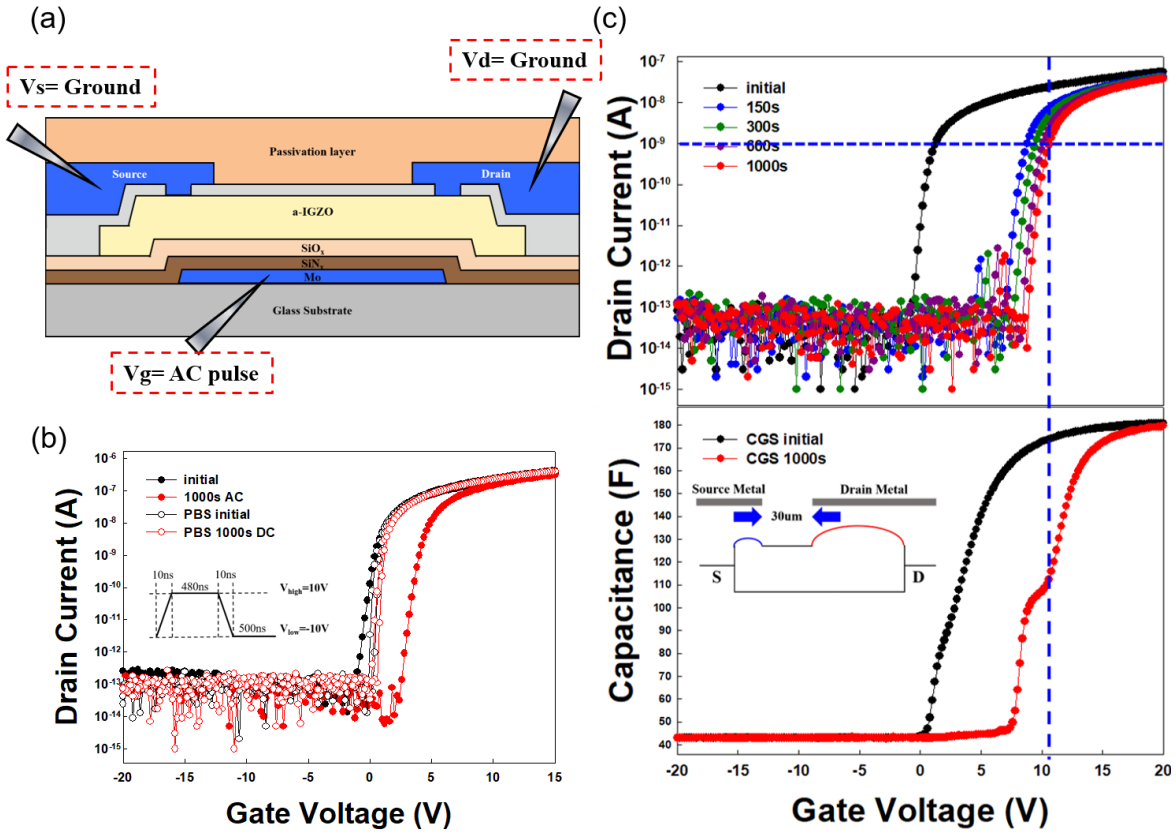

Figure 2 – (a) Cross-section of etching-stop layer a-IGZO TFT (b) Transfer characteristic curve of before and after both AC and DC PBS (c) Transfer characteristic curve of asymmetric source/drain metal after 1000s AC PBS stress. The blue line indicates the turn on voltage of Id-Vg matches to the turn on of C-V curve.

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EFFECT OF DIFFERENT A-InGaZnO TFTs CHANNEL THICKNESS UPON SELF-HEATING STRESS

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Key Words: Indium-Galium-Zinc-Oxide, Self-Heating Stress, Channel Thickness, Charge Trapping

In this work, Indium-Galium-Zinc-Oxide Thin Film Transistors (IGZO TFTs) with different channel thickness has been compared after self-heating stress (SHS). In previous literatures, self-heating of TFTs has been widely discussed and Joule Heat caused during driving TFTs has been compared with different channel length and width [1]. However, different channel thickness hasn't been investigated. Although TFTs with a larger channel thickness possess a greater drain current, a less degradation is observed when comparing with small channel thickness structures, demonstrated in Figure 1(a). The ΔVt shift in the transfer characteristics are well described by the stretched-exponential equation. The E_T value, which is the average effective barrier height for electron transport, is extracted in Figure (b). Results has shown that in the thick IGZO TFTs, the value is almost twice of that in the thin IGZO TFTs. From COMSOL simulations demonstrated in Figure 1(c), in could be noticed that different channel thickness effects the electrical field locating at the gate insulator. Therefore, a model is proposed to explain the degradation difference, illustrated in Figure (4).

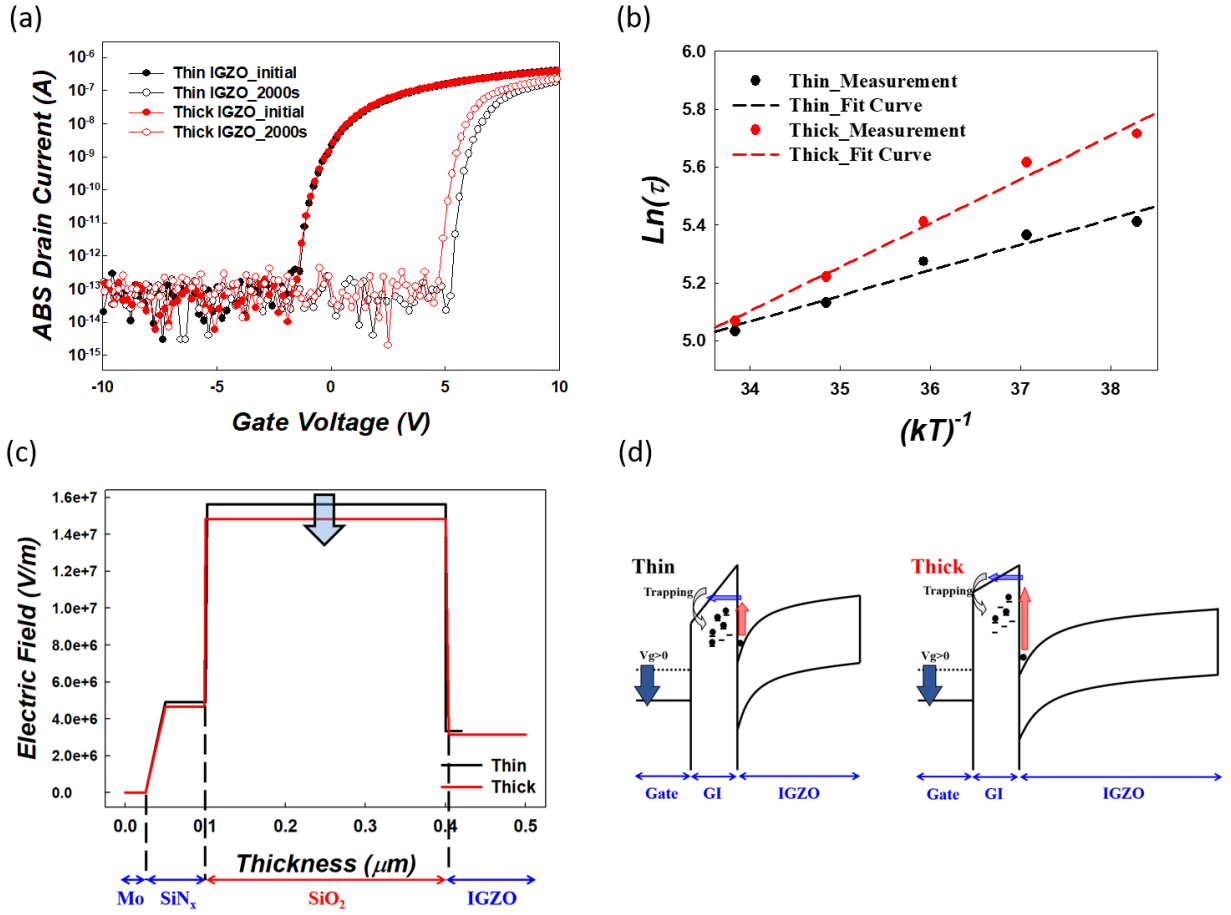

Figure 3 – (a) Transfer characteristics of two different channel thickness in a-IGZO TFTs (b) Time constant τ as a function of reciprocal temperature (c) Simulation of electrical fields by COMSOL (d) The schematic diagram of different channel thickness during charge injection between the channel and gate insulator

Reference:
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MECHANISM OF THERMAL FIELD AND ELECTRIC FIELD IN RESISTIVE RANDOM ACCESS MEMORY USING THE HIGH/LOW-K SIDE WALL STRUCTURE

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Key Words: RRAM, scaled down, forming voltage, thermal conductivity, electrical field

In the Internet of things (IoT) era, low power consumption memory will be a critical issue for further device development. Among many kinds of next-generation memories, resistive random access memory (RRAM) is considered as having the most potential due to its high performance. To prevent unrecoverable hard break-down of a RRAM device, the RRAM should be collocated with a transistor for external current compliance. With decreasing device cell size, however, the operating voltage of the transistor will become smaller and smaller. Previous study has determined that the forming voltage of RRAM increases when device cell size is reduced, which is a very crucial issue especially when the device is scaled down. We have proposed a high-k sidewall spacer structure in RRAM to solve the dilemma of increasing forming voltages for device cell scaling down. Based on the COMSOL-simulated electrical field distributions in the high-k RRAM. In addition, thermal conductivity of sidewall spacer influenced resistive switching behavior. Suitable thermal conductivity of sidewall materials can enhance resistive switching behavior.

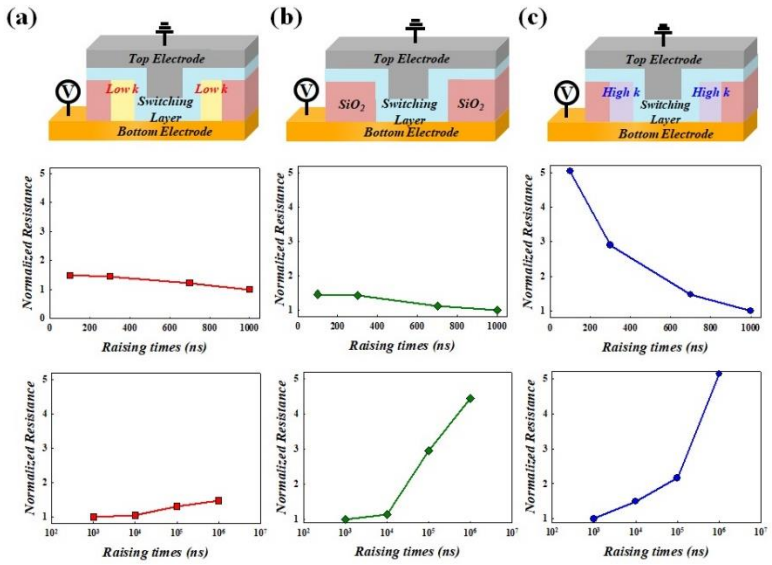

Figure 4 – Increasing forming voltage of scaling down is solved by varying permittivity of the switching layer. Three devices were fabricated by RF-sputter, including (a) Low-k, (b)SiO_2 and (c)High-k side walls. After applying reset process with fast IV of Waveform Generator/Fast Measurement Unit (WGFMU), the trend of HRSs of low-k and SiO_2 side walls was slowly, and the trend of HRSs of high-k side walls increased during the rising time decreasing. As rising time increased between 1us to 100us, the trend of SiO_2 and high-k side walls was upward. In contrast, the trend of low-k side wall was slowly.

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INFLUENCE OF ELECTRODE THERMAL CONDUCTIVITY ON RESISTIVE SWITCHING BEHAVIOR DURING RESET PROCESS

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Key Words: Thermal conductivity, Active oxygen ions, Reset process, Effective switching gap, RRAM.

Resistive random access memory (RRAM) is the most promising candidate for non-volatile memory (NVM) due to its extremely low operation voltage, extremely fast write/erase speed, and excellent scaling capability. However, an obstacle hindering mass production of RRAM is the non-uniform physical mechanism in its resistance switching process. This study examines the influence of different electrode thermal conductivity on switching behavior during the reset process. Electrical analysis methods and an analysis of current conduction mechanism indicate that better thermal conductivity in the electrode will require larger input power in order to induce more active oxygen ions to take part in the reset process. More active oxygen ions cause a more complete reaction during the reset process, and cause the effective switching gap (dsw) to become thicker. The effect of the electrode thermal conductivity and input power are explained by our model and clarified by electrical analysis methods.

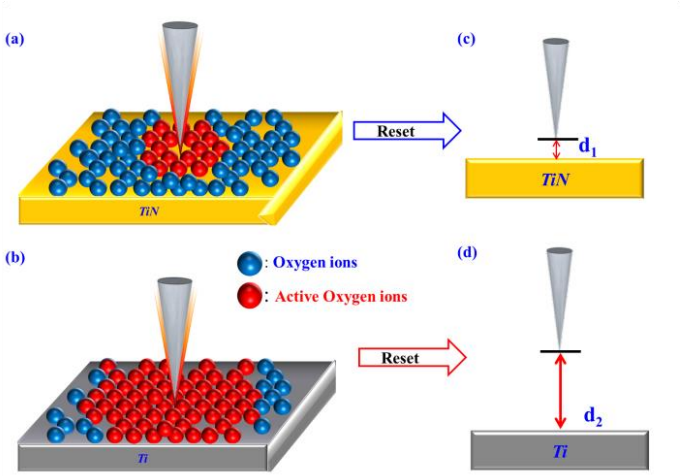

Figure 4. The physics mechanism schematic diagram (a) The quantity of active oxygen ions which can progress the redox reaction for the TiN switching active device (which is effectively induced by the heat) is less. (b) In the Ti switching active device, the quantity of active oxygen ions and the demand for input power are more for the Ti switching active device. (c) The lower quantity of active oxygen ions induces a thinner effective switching gap (dsw) after the reset process. (d) The higher quantity of active oxygen ions induces a thicker effective switching gap (dsw) after the reset process.

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THE RELIABILITY OF AMORPHOUS-InGaZnO THIN FILM TRANSISTOR INFLUENCE BY SELF-HEATING STRESS AT HIGH TEMPERATURE UNDER COMPRESSIVE STRAIN

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Key Words: Flexible a-IGZO TFT, Mechanical bending stress, Abnormal hump

Flexible thin-film transistors (TFTs) play an important role in flexible technology applications, including wearable devices and high-resolution foldable displays and as curved displays. A reliability test was performed in this work, including mechanism and electrical stress at high temperature. An abnormal hump can be found in flexible a-$InGaZnO_4$ TFTs after a self-heating stress at 90°C under compressive bending. COMSOL simulation confirmed that the etching stop layer absorbs more mechanism stress than the gate insulator. Accordingly, during the reliability stress, holes induced by the impact ionization tend to inject into the defect in the etching stop layer near the source side rather than the gate insulator, which is induced by compressive bending. Single side C-V measurement and forward/reverse-operation mode are utilized to analyze the hole trapping distribution.

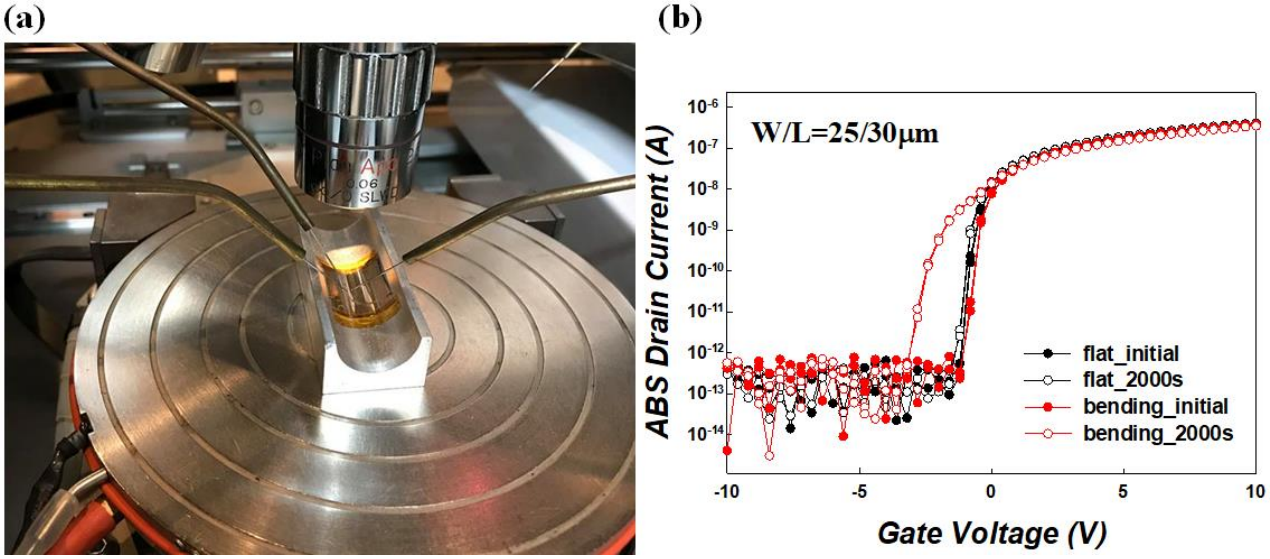

Figure 5 – (a)Photo of flexible a-IGZO TFT under measurement. (b)I_D-V_G transfer characteristics with V_D=0.1V for devices undergoing width-axis compression bending.

ANALYSIS OF IGZO CRYSTALLINE STRUCTURE AND ITS STABILITY BY FIRST-PRINCIPLES CALCULATIONS

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Key Words: oxide semiconductor, IGZO, first-principles calculation

In-Ga-Zn oxide (IGZO), an oxide semiconductor, has been actively researched as a semiconductor material having features different from those of silicon in recent years [1]. IGZO is used as a transistor material in backplanes of commercially available displays. Transistors including crystalline IGZO have high stability and thus are suitable for mass production [2].

Our previous studies revealed that the selected area diffraction pattern of an IGZO film formed at room temperature by sputtering is a halo pattern, whereas diffraction spots are observed in the diffraction pattern obtained by nanobeam electron diffraction with a probe diameter of 1 nm [3,4]. These results suggest that the IGZO film has rather nanometer-sized crystalline structures than a completely amorphous structure. We named this film “nano-crystalline IGZO (nc-IGZO) film.” Other researchers have reported that the nc-IGZO film has a crystalline-cluster composite structure, according to the analysis results obtained by grazing-incidence X-ray diffraction, anomalous X-ray scattering, and reverse-Monte-Carlo simulation [5].

In this study, an IGZO structure having a minute crystalline region, which was considered to exist in nc-IGZO as a local structure, was created by first-principles calculations and its stability was analyzed. The IGZO model having a crystalline region used in this study was obtained by a melt-quench method in the following manner. Note that the initial structure had a hexagonal-prism crystalline region at the center and an amorphous region (random atomic arrangement) around the crystalline region. The composition ratio was In:Ga:Zn:O = 1:1:1:4 and the density was 6.1 g/cm^3. First, for structural relaxation with the crystalline region maintained, the amorphous region was fused in quantum molecular dynamics simulation (3500 K, 6 ps) while the atomic arrangement of the crystalline region was fixed, and the structure was cooled to 500 K at a rate of 500 K/ps and held at 300 K for 5 ps. Finally, the entire structure including the crystalline region was optimized towards the target structure (Fig. 1). An amorphous model was also created for reference. The amorphous model was obtained by quantum molecular dynamics simulation of the entire structure under similar temperature conditions without fixing the atomic arrangement of the crystalline region, followed by structural optimization. The comparison between the two models showed that the total energy of the IGZO model having a crystalline region was lower than that of the amorphous model (not having a crystalline region). This suggests that the crystalline region contributes to structure stabilization.

For more detailed thermal stability analysis of the IGZO structure having a crystalline region, quantum molecular dynamics simulations were performed at several temperatures. The results will be available at the conference.

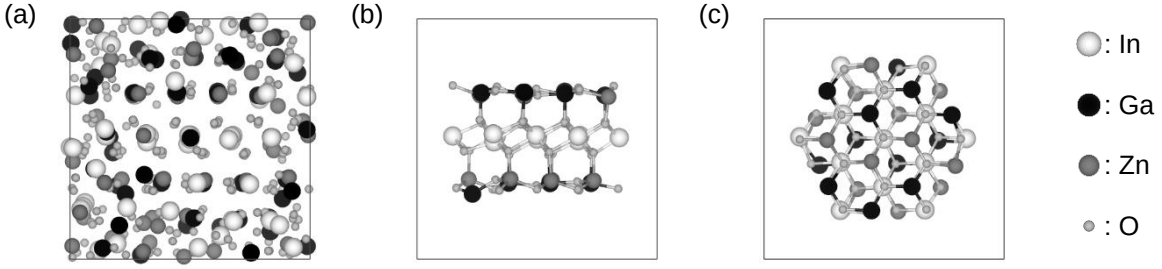

Figure 1 – The model having a crystalline region obtained by first-principles calculations: (a) the entire structure; (b) a portion initially set as a crystalline region; and (c) a 90° rotated view of (b).

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Bi-DIRECTION TRANSMISSIBLE GATE DRIVER ON ARRAY

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1. Background

In recent years, gate driver using amorphous silicon (a-Si) technology for the TFT-LCD has become the main stream due to the mature manufacturing, low-cost processing, and elimination of the gate driver ICs [1],[2]. However, it's still three challenges of design the integrated gate driver by a-Si encounters which are the low field-effect mobility, low reliability issue under high voltage stress, and the lack of P-type transistor.

2. Operation of the proposed circuits

Figure 1 shows the circuit schematic and correlated timing diagram. In the proposed circuit, VGH (Voltage Gate High) and VGL (Voltage Gate Low) are defined as VDD and VSS , respectively. The clock signals are four non-overlap different phases, which means the proposed circuit is driven by 25% duty cycle clock. In forward transmission event, we designate VDD_F as VDD and VDD_R as VSS. If there is a requirement for backward transmission event, first is to reverse the clock order, and re-designate VDD_F as VSS and VDD_R as VDD. Second is to input the start pulse (VSTART)to trigger the last stage (Stage[n]). Then, the stages in the gate driver could operate in backward sequence.

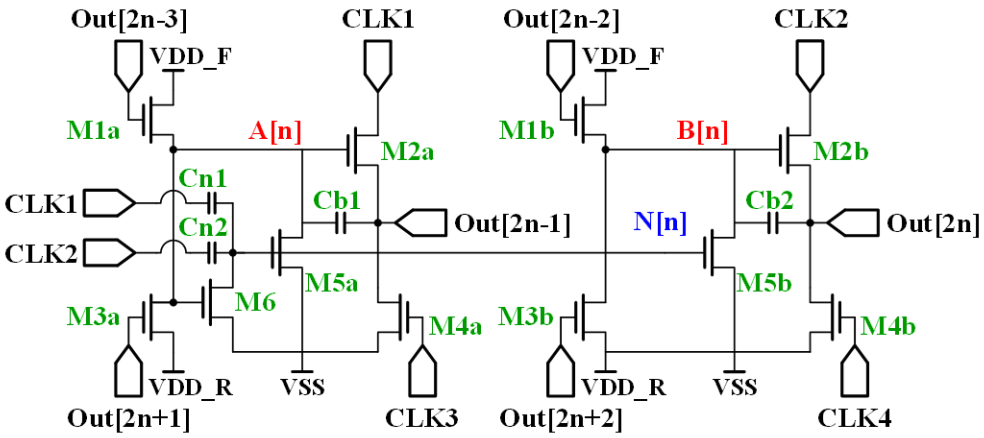

Fig. 1 The circuit schematic

A TCAD CALIBRATED APPROACH FOR ON-STATE MODELING OF AMORPHOUS OXIDE SEMICONDUCTOR TFTS

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Key Words: amorphous oxide semiconductor, IGZO, TFT, band-tail states, short channel effects

Amorphous oxide semiconductor materials such as IGZO exhibit electrical characteristics that are not well represented by conventional device models due to the presence of band-tail states (BTS). Common parameters such as threshold voltage and channel mobility that are extracted from measured electrical characteristics can be misrepresentative due to discrepancies between the device operation and the chosen operational model. Compact models that have been developed for model accuracy and circuit simulation efficiency offer limited insight on the underlying device physics involved. The focus of this work is a model for device engineering which maintains a close physical connection to device operation, and captures the 2D influence of both the gate and drain bias conditions on the ionization and deionization of acceptor-like BTS near the conduction band edge.

A device model for the on-state operation of accumulation-mode IGZO TFTs was recently presented as an adaptation of a Level 2 SPICE (L2S) model [1]. The model introduced channel charge adjustments which account for the occupancy of BTS as influenced by the gate and drain voltage, and provided an exceptional match to both simulated and measured device characteristics. However the integrity of the model as assessed by the ability to discriminate between the influence of BTS and short-channel effects (SCE) was compromised as the device channel length was decreased. Accumulation-mode devices are susceptible to the onset of SCE at relatively long channel lengths due to the lack of a source-channel junction barrier. While the subthreshold region may show minimal influence of drain induced barrier lowering (DIBL), the on-state may exhibit an effective V_T decrease in the triode region of operation.

A new model is presented which incorporates this on-state DIBL along with channel length modulation, and demonstrates improved discrimination between BTS and SCE in the model fit at device channel lengths L ≥ 3 µm. Silvaco® Atlas™ TCAD played a key role in device model development. A long-channel reference device was used to establish the impact of SCE on short devices, which was then modeled by ΔV_T and □ terms in associated triode and saturation regions of operation. For channel lengths L < 3 µm, a lumped SCE multiplier was used to represent short-channel behavior, followed by the application of BTS parameters for channel charge adjustments. Modeling results derived from both simulated and measured TFT characteristics will be presented.

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EFFECTS OF X-RAY IRRADIATION ON THE NOISE BEHAVIOR OF LOW-TEMPERATURE POLYCRYSTALLINE SILICON TFTS

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Key Words: Low-temperature polycrystalline-silicon, X-ray, low frequency noise, thin film transistors (TFTs)

X-ray active pixel sensor (APS) has attracted great attention because of higher signal to noise ratio (SNR) by amplifying the signal in pixels. Each APS circuit contains the X-ray detector and a-Si thin film transistors (TFTs). Due to the high mobility, low-temperature polycrystalline- silicon (LTPS) TFTs have been proposed as a suitable candidate to replace the a-Si TFT. Previous research revealed that the significant transfer curve change under X-ray irradiation can be observed. However, the effects and reliability of X-ray irradiation on the low frequency noise (LFN) are rarely discussed. In order to find out the noise behavior of LTPS TFTs under X-ray, we investigate the noise spectrum density of the LTPS TFTs under irradiation conditions in this paper.

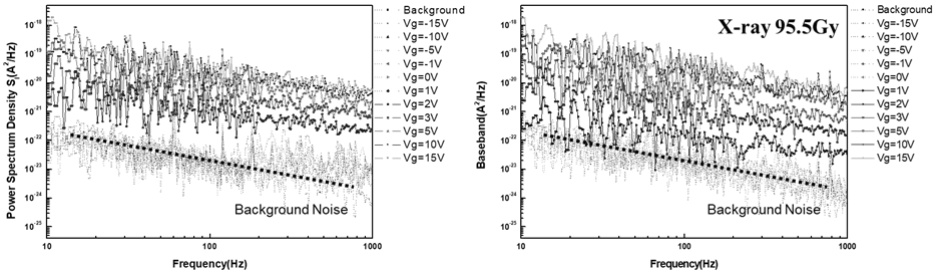

Figure 6 –Power spectrum density of LTPS TFTs measured at different V_G from -15 to 15 V and a constant V_D of 9 V (a) in dark and (b) after X-ray of 95.5mGy

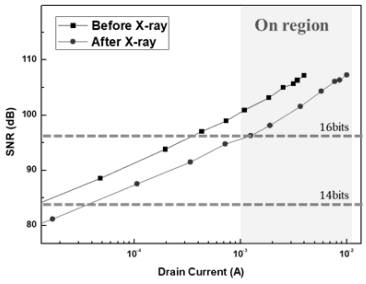

Figure 3 –The curves of SNR in dB scale versus I_D in logarithm scale for the LTPS TFTs before and after X-ray irradiation

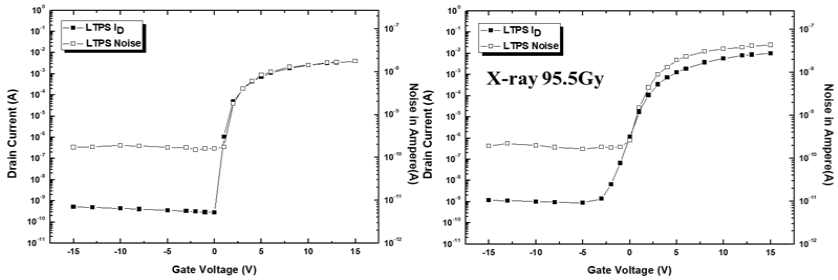

Figure 2 –Dependences of ID and NiA on VG for the LTPS TFTs (a) in dark and (b) after X-ray of 95.5mGy

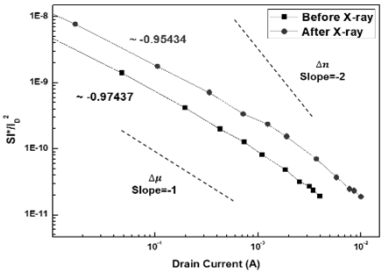

Figure 4 –The curves of S_I*/I_D^2 versus I_D for the LTPS TFTs before and after X-ray irradiation

The results of LFN power spectrum density (S_I) versus the frequency (f) measured with and without X-ray irradiation are shown in Fig. 1(a) and 1(b). The results indicated that the level of power spectrum density move upward with the irradiation. And then, we try to analyze the LFN behavior in another approach by using NiA, which is an index to represent the noise in ampere in our previous paper [1], as shown in Fig. 2(a) and 2(b). In the APS application, the best SNR which a TFT can provide is expected as the ratio of signal power to the noise power. Therefore, Fig. 3 shows the SNR in dB scale versus log (I_D). We can observe that SNR after X-ray irradiation decreases by 5dB. Besides, The normalized noise power spectrum integral S_I*/I_D^2 versus I_D before and after X-ray irradiation are plotted in Fig. 4. The slopes of the curves are around -0.97 and -0.95, which is more close to -1 for the model of mobility fluctuation. It is further revealed that the noise mechanism under X-ray is attributed to mobility fluctuation [2].

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RELIABILITY OF PLASMA-ETCHED COPPER LINES ON A GLASS SUBSTRATE

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Copper (Cu) thin films can be etched into 0.3 micrometer Cu patterns, as shown in Figure 1. This process has been used in the fabrication of large-area thin film transistor (TFT) arrays for LCDs, interconnect lines in high density BiCMOS circuits, and source, drain and gate electrodes of a-Si:H TFTs (1,2). The reliability of the Cu line is usually investigated with the isothermal electromigration (EM) method (3).

In almost all studies, the Cu line was prepared on the silicon substrate coated with a dielectric layer. There are few studies on Cu line lifetime on the glass substrate. Also, the EM failure investigation was focused on the line broken time, which could be influenced by the edge roughness, step coverage, current density, etc. (4). The physical and structure changes of the Cu line during the EM stress time are often neglected (5). In this paper, authors discuss the application of the plasma etched Cu line for the SSI-LED array. It allows the driving of the individual device for light emitting at specified conditions, which enables applications in displays, optical interconnects, etc. The transformation of the Cu line from a continuous pattern to the broken state will be reviewed. The temperature change with respect to the stress current density and the lifetime will be discussed. In summary, the room temperature plasma-based Cu etch process can be applied to a wide range of electronic and optoelectronic products. The understanding of the reliability of the Cu line is important for these applications.

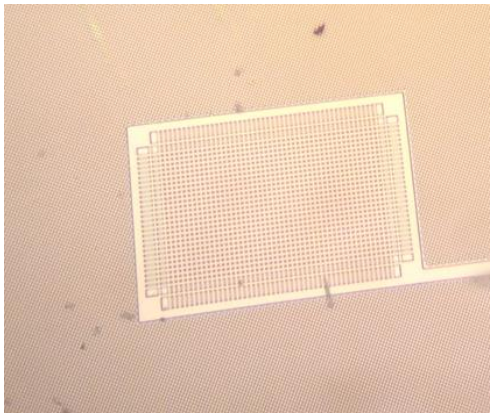

Fig. 1. 0.3 micrometer Cu pattern etched with the plasma-based process.

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GRAVITATIONAL LEVEL EFFECTS ON OPTICAL PROPERTIES OF ELECTRODEPOSITED ZnO NANOWIRE ARRAYS

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The coupling phenomena between the interfacial reaction rate and the microstructural/morphological variation rate must be reasonably well controlled to fabricate nano/meso- structural devices in a large scale. Otherwise, the physical property uniformity inside the device is not guaranteed to lose its superiority in the market. Free standing ZnO nanowire array was successfully synthesized on ITO/FTO substrate by template-free method in $Zn(NO_3)_2$ aqueous solutions. Two types of electrode configurations were employed in order to quantitatively examine the effect of gravitational strength on electrodeposited ZnO nanowire array: (a) a horizontal cathode surface facing downward over an anode (C/A) and (b) an anode over a cathode (A/C). The former configuration may simulate the microgravitational environment, because macroscopic natural convection is not induced. PL of ZnO nanowire array was measured. More uniform nanowires are synthesized in C/A configuration than in A/C. Seeding ZnO nanoparticles on ITO/FTO substrate can control the diameter as well as the orientation.

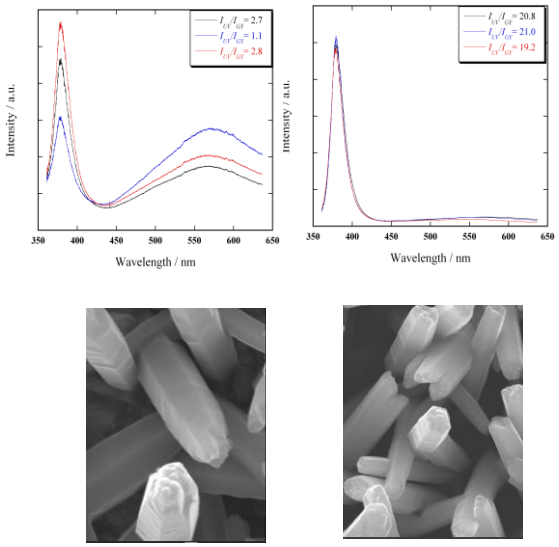

Figure (a)PL spectra from ZnO electrodeposited in Aq. Solution

(b) SEM images of electrodeposited nanowire
(left)A/C , (right)C/A

A PIECEWISE LINEAR APPROXIMATION FOR OUTPUT CHARACTERISTIC FOR SHORT-CHANNEL "EXTRINSIC" MOSFET WITH ACCOUNTING OF NONZERO DIFFERENTIAL CONDUCTANCE IN SATURATION REGIME AND SOURCE PARASITIC RESISTANCE EFFECT AT HIGH DRAIN BIASES

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Key Words: MOSFET, contacts resistance, differential conductance in saturation regime, saturation effect of charge-carriers drift velocity, compact modeling

Previously, we transformed the linear drain bias asymptote equation for the MOSFET drain current in the saturation regime from the "intrinsic" (without accounting for the contact and parasitic series resistances) case into "extrinsic" (with accounting for the contact and parasitic series resistances) case with accounting for the velocity saturation effect. As a result, we obtained the equation for the drain current that yielded the nonlinear dependence on the "extrinsic" drain bias for the short-channel "extrinsic" MOSFET in saturation regime in an implicit form. This equation can be solved numerically in the entire range of the "extrinsic" drain bias. Using this extrinsic equation, we derived the equation for the differential conductance of the "extrinsic" MOSFET at the "saturation point". Such "saturation point" is determined by the saturation current and saturation voltage equations for the "extrinsic" MOSFET that are well known from literature. We proposed a linear approximation for the dependence of the short-channel "extrinsic" MOSFET drain current on the "extrinsic" drain bias in the saturation regime. This approach works well for not very high drain bias.

In this paper, we analyze the previously obtained nonlinear equation for the short-channel "extrinsic" MOSFET drain current I_d and derive for one the asymptotic value V_{gt} / R_S for the "extrinsic" drain bias V_{ds} tending to infinity. Here V_{gt} is the "extrinsic" gate-to-source bias centered on threshold voltage and R_S is the source parasitic resistance. Note, that in this asymptotic case "intrinsic" centered gate-to-source bias ($V_{GT} = V_{gt} - I_d R_S$) tending to zero. Finally, we propose a piecewise linear approximation for the drain current dependence of a short-channel "extrinsic" MOSFET on the drain-to-source bias. This dependence includes the linear triode regime, the linear saturation regime and the regime with constant asymptotic drain current due to source parasitic resistance effect at high drain biases. We also suggest an approach for smoothing this piecewise linear approximation. These results can be applied for other types of field-effect transistors, like thin-film transistor (TFT) and organic field-effect transistor (OFET), as well. Thick solid line on Figure 1 - a piecewise linear approximation for short-channel "extrinsic" MOSFET drain current dependence on drain-to-source bias ($V_{gt} / V_L = 2$, $R_S \times \beta \times V_L = 5$, $R_D \times \beta \times V_L = 2$, $\alpha = 1.1$, $\lambda \times V_L = 1$). Here V_L - characteristic voltage, related to the drift velocity saturation in high electric field, β - MOSFET transconductance parameter, α - dimensionless saturation parameter, λ - channel-length modulation parameter, R_D - drain parasitic resistance. Thin solid lines – saturation current and saturation voltage levels. Dashed line – numerical solution of the equation for the drain current that yields the nonlinear dependence on the "extrinsic" drain bias for the short-channel "extrinsic" MOSFET in saturation regime. 2 dots 1 dash – exact solution without accounting for the velocity saturation effect. In this case we have cubic equation with respect to "intrinsic" centered gate bias V_{GT}. 2 dots 3 dashes - solution of quadratic equation obtained from cubic one with neglected cubic term, that is good approximation with V_{GT} tending to zero while V_{ds} tending to infinity.

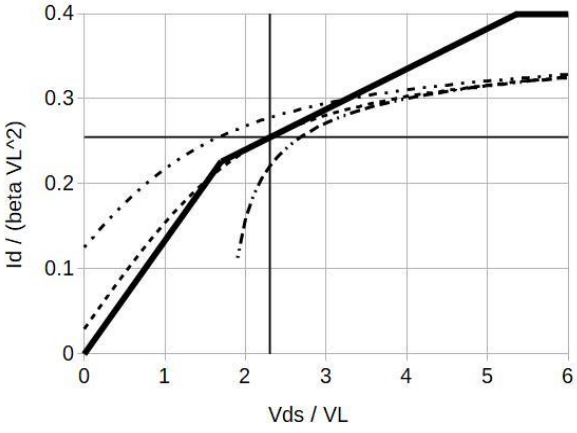

Figure 7 – A piecewise linear approximation for short-channel "extrinsic" MOSFET drain current dependence on drain-to-source bias