TRANSPARENT OXIDE SEMICONDUCTORS: MATERIALS DESIGN, ELECTRONIC STRUCTURE, AND DEVICE APPLICATIONS

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In 1995, I presented a materials design concept for transparent amorphous oxide semiconductors with a large electron mobility (TAOS) at the 16th International conference on amorphous semiconductors along with concrete example materials of TAOS and the paper was published in 1996 [1]. The basic concept of TAOS is that large electron mobility should be retained even in amorphous materials if the conduction band minimum is mainly composed of spatially large spread of metal ns-orbitals.[1] The validity of this design concept was demonstrated by analysis of electronic structure using photoemission experiments combined with calculations based on X-ray structural analysis [2]

In 2003 we reported high mobility TFTs (~80cm^2/Vs) using epitaxial thin films of InGaZnOx (IGZO) in Science [3] , and fabricated amorphous IGZO on plastic substrates in Nature with expectation for application to backplanes of flexible OLEDs [3]. The TFT mobility is ~10cm^2/V-s, which is larger by an order of magnitude than that of hydrogenated amorphous Si(a-Si:H). Since TAOS-TFTs can be easily fabricated on various types of substrates at low temperatures by conventional sputtering method and their mobility is 10-30$cm^{2/}$V-s.

IGZO-TFTs, which have been most extensively studied to date [5], are now used to drive displays for high precision LCDs and large-sized (55 and 65inches) OLED-TVs. Amorphous oxide semiconductor TFTs appears to be advantageous to drive large-sized OLEDs with respect to scalability, homogeneity and production cost. However, various technical issues still remain to be resolved when oxide TFTs are adopted as the driving transistors in OLEDs; currently applied small OLEDs are driven by p-channel LTPS-TFT using normal stacking structure (cathode top). Since oxide TFTs work only as n-channel, the device stacking sequence are required to be reverse with respect to stability and image clarity. There is an obstacle to realize inverted OLEDs which has performance comparable to that of conventional normal-type OLEDs, the absence of appropriate electron-injection and transport materials. We have developed new TAOS for this demand; amorphous C12A7:e [6] for e-injection and ZnO-based new TAOS for e-transport[7]. Both materials can form Ohmic contact with conventional cathode metals (ITO and Al). The inverted OLEDs fabricated using this material combination exhibit comparable or superior to that of conventional normal type device using Al/LiF cathode.

In this talk, I review the progress in oxide semiconductors for display application covering materials design concept and new materials for NBIS instability-free TFTs [8] and OLEDs

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ULSI AND TFT TECHNOLOGIES IN INDUSTRY, RESEARCH AND HIGHER EDUCATION IN FRANCE: AN EVOLUTION TOWARDS INNOVATION RESULTING FROM CLOSE AND SUSTAINABLE INTERACTION

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Key Words: Large area electronics, Thin Film transistors, ULSI, Higher education, technology evolutions.

The semiconductor industry and associated microelectronic production began in France in the early 1980s as part of the national microelectronics plan launched by the French government to meet the needs of new economic sectors that are heavy users of microelectronic products. Indeed, microelectronic circuits, devices and systems are the key elements of the information technology field, which includes computer and communications capabilities, and application fields such as aerospace, transport, and energy, mainly. Several new technologies had to be developed, corresponding to the first advent of communication tools such as Minitel (ancestor of the web) or credit cards, which then underwent huge development. This implied a major effort on both integrated silicon technologies and large area electronics technologies oriented flat panel displays on glass substrates (low temperature process). The latter were to replace the cathode ray tube. Let us notice that due to the drastic reduction of dimensions in ULSI technologies, the thermal budget significantly decreased and both technological approaches progressively converged; today, many deposition techniques are common, for example.

In parallel with the major effort towards the microelectronics industry, the French government has decided to improve higher education in this field and to train future engineers, masters and doctors in research and development and manufacturing with the corresponding knowledge and know-how. More recently, a new national plan has been launched by the French “Commissariat aux Grands Investissements” (Future Invest Plan or PIA1) to improve large area and integrated technologies and adapt to the digital society of the future. This focuses on connected objects and the Internet of Things, products that mainly combine the different components of the fields of microelectronics [1] and more particularly integrated technologies, embedded electronics and large area technologies suitable for flat panel displays, sensors and actuators, but also components of other domains linked to their applications. This supposed also multidisciplinarity [2].

As a consequence, the training of graduate students must follow this evolution in order to well meet the needs of companies and research laboratories with a clear orientation towards innovation. A specific French national program was launched in 2011 and entitled IDEFI for Excellence Initiative for Innovative education in order to set-up innovative formations that may correspond to new pedagogical approach and new content of curricula adapted to the new technologies. The French national network in microelectronics, CNFM [4], applied and succeeded with the project entitled FINMINA [5] for Innovative training in microelectronics and nanotechnologies. With the advent of new educational technologies based mainly on online training such as MOOCs, the strategy has focused on the know-how part of learning. The 12 common centers of the French microelectronics network (CNFM), which include numerous design platforms, cleanrooms, and characterization and testing platforms, have engaged in innovative training projects covering all microelectronics sectors, targeting future applications of connected objects and the industry 4.0.

After a presentation of the context of microelectronics and the evolution of ULSI and TFT technologies, both in academic research and industrial environments, the paper highlights the strategy developed by the French academic and microelectronics community around innovation. Examples of the development by students of future integrated components up to the nanoscale, system-on-chip combining integrated and large area technologies will be presented. The ultimate objective is to best meet the societal needs of the 21st century.

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TERAHERTZ TESTING OF VERY LARGE SCALE INTEGRATED CIRCUITS

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Growing sophistication of electronics devices and circuits and, especially of VLSI and ULSIC, presents increasing demands on circuit testing and fault diagnosis. The conventional well-established technique of electric AC and DC testing is costly, does not assure a complete fault identification. This technique also presents an additional security problem making it possible to design faked circuits avoiding the identification by this testing.[1] Fabrication of and even perception of faked VLSI capable of surreptitious performance has become an increasing problem often referred to as “trojan hardware”. Experimental techniques, such as laser scanning[2]and terahertz imaging [3-5] have a limited resolution signal-to-noise ratios and encounter difficulties in defect identification. A new approach of THz testing of Microwave Monolithic Integrated Circuits (MMICs)[6], VLSI, and ULSIC is based on measuring the circuit responses at the pins or input/output leads and comparing these responses with etalon responses. [7, 8] This technique could augment or replace the electrical testing and/or laser and THz scanning testing for production testing, burn-in testing, high temperature testing, and infant mortality testing. It could also be extended for the fault diagnosis and identification and for the lifetime and reliability predictions. To this end it could be augmented by the low noise measurements. The number of the detected responses could be very large, since the permutations of the voltages between the pins and leads could be measured at the different positions of the scanning THz beam, different THz frequencies and polarizations, in the pulsed and/or CW mode, at the different modulation frequencies and at the different THz intensities. This technique could be used under or without bias. The processing of these responses forming multi-dimensional images in the excitation parameter space could be processed using artificial intelligence algorithms and machine learning approaches making this testing technique self-learning and self-improving. This testing could be further improved by designing for testability by THz responses at the pins.

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PHOTOEMISSION CHARACTERIZATION OF INTERFACE DIPOLES AND ELECTRONIC DEFECT STATES FOR GATE DIELECTRICS

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Key Words: Photoemission, Interface Dipole, Defect States, Dielectrics

In the development of Metal-Insulator-Semiconductor (MIS) devices, gate dielectric technology is of great importance and includes major scientific and technological issues to be solved for required device performance and reliability [1]. In particular, characterization of electronic defects in dielectrics and at their interfaces with semiconductor substrates as well as energy band profiles has been imperative to gain a better understanding of physics of dielectric/semiconductor heterostructures [2, 3].
In this work, our recent achievements on the characterization of gate dielectrics and their stacked interfaces by means of photoemission techniques have been reviewed. First, we have shown how valuable the cut-off energy of photoelectrons is to measure directly the potential change due to electrical dipoles at the interface in stacked dielectrics [4]. And then, we have demonstrated how powerful total photoelectron electron yield spectroscopy (PYS) [5, 6] is to quantify the energy distribution of electronic defect states in gate dielectrics and at dielectric/semiconductor interfaces.
The inner potential changes in dielectric stacks reflect in changes in the cut-off energy of secondary photoelectrons (SEs) measured in high-resolution x-ray photoelectron spectroscopy (XPS) [4]. After calibration of the kinetic energy of core-line signals from the underlying layer, an abrupt potential change due to electrical dipoles at the interface between dielectrics, resultant abrupt potential change can be measured as a change in the cut-off energy of SEs. The observation of cut-off energy provides us an advantage in simple and precise evaluation of the potential change due to electrical dipoles as compared to a discussion on dipole formation based on the energy shift of core-line signals which reflects not only the potential change due to dipoles but also the chemical shift, that is, change in the chemical bonding features. From SE spectra near the lowest limit in kinetic energy for the samples before and after the formation of various high-k dielectrics on thermally-grown thick SiO_2, we found that, with the formation of either ultrathin Al_2O_3 or HfO_2 or TiO_2 on SiO_2, the cut-off energy of SEs was shifted toward the higher kinetic energy side. On the other hand, in the cases of Y- and Sr-oxides with silicate formation at the interfaces, a slight opposite energy shift was detected. The analyses of the core line signals confirm that there is a linear correlation between the observed potential changes and the ratios in the oxygen anion density at the interfaces between SiO_2 and high-k dialectics as suggested in Ref. [8].
In the photoelectron yield measurements, the total number of photoelectrons emitting from the sample is counted considering the incident photon flux, the yield spectrum is related to an integral over the occupied density of states existing near the sample surface [5, 6]. From photoelectron yield spectra of 2nm-thick SiO_2 formed 500ºC by remote plasma enhanced CVD on n-type GaN(0001) before and after N_2 anneal at 800ºC, we found that, with the N_2 anneal at 800ºC, the yield from the defects was reduced markedly. The 1st derivative of the measured yield spectrum with respect to incident photon energy leads us to the energy distribution of occupied defect state densities in consideration of density of states of the GaN valence band, measured photoelectron yield from the GaN VB and photoelectron escape depth. As a result, occupied states are reduced down to ~$1x10^{11}cm^{-2}eV^{-1}$ at the energy corresponding to the midgap of GaN near the SiO_2/GaN interface with the N_2 anneal at 800ºC. The defect state density near the conduction band edge, which was crudely estimated in consideration of electron occupation probability based on the Fermi-Dirac distribution, is in good agreements with the result obtained from the capacitance-voltage (C-V) analysis using the Terman method [7]

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WHAT WILL COME AFTER V-NAND – VERTICAL RESISTIVE SWITCHING MEMORY?

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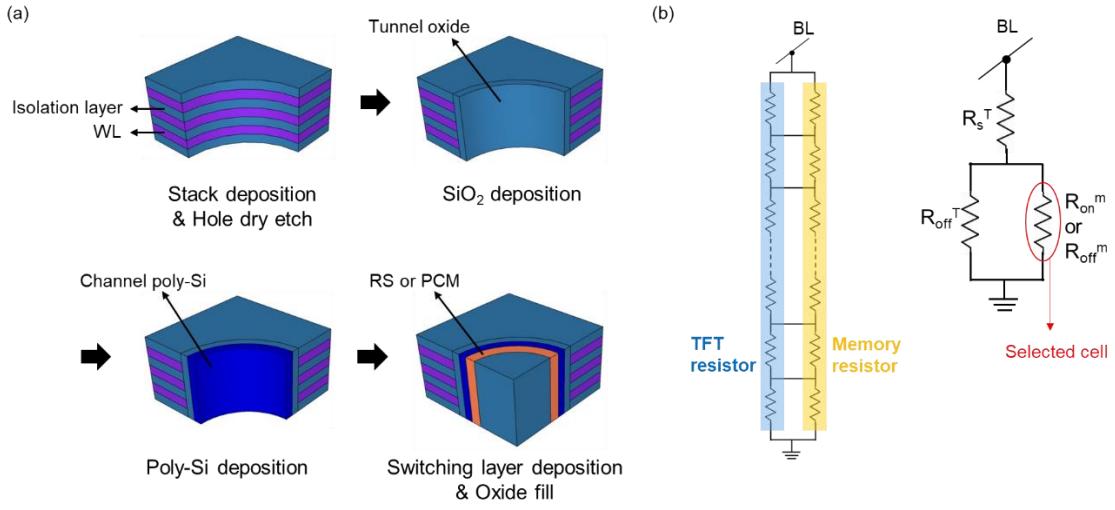
Key Words: Vertical NAND flash; scaling; resistive switching memory; architecture; oxide semiconductor

The NAND flash memory serves as the key enabler of the flourishing of portable handheld information devices, such as the cellular phone. The recent upsurge in the sales of vertical NAND flash memory (V-NAND) entails a further increase in the available information capacity at the edge devices and the servers with higher performance and lower power consumption compared with the magnetic hard-disc drives. Nonetheless, there will certainly be an upper limit for the number of stacked layers, which will be the point at which further memory density increase will stop. While V-NAND is a supreme outcome of semiconductor memory technologies, it still relies on conventional Si-based materials. The newly explored memory materials and concepts, such as the resistance-based memories, can, therefore, be an appealing contender to or successor of V-NAND. In this talk, the current state of V-NAND is first briefly looked into, and then the eventual limitation of memory density increase and performance boost are discussed. Most importantly, the possible strategies of integrating the resistance-based memories into the vertical architecture are then discussed. Among them, V-NAND-like vertical resistance-switching random access memory will be focused. The figure below shows the schematic diagram for this type of vertical device (a), and its equivalent circuit diagram (b). For this application, higher performance of channel material, other than the current amorphous-like Si, is necessary. For such purpose, the programming characteristics of charge trap flash memory device adopting amorphous $In_2Ga_2ZnO_7$ (a-IGZO) oxide semiconductors as channel layer were evaluated, where the a-IGZO thin film was grown by either metal-organic chemical vapor deposition (MOCVD) or RF-sputtering processes. The MOCVD film showed superior performance to the sputtered film, perhaps due to the involvement of the appropriate level of hydrogen.



OPERATION ANALYSIS OF RESISTIVE SWITCHING OF CBRAM USING IN-SITU TEM

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Key Words: Resistive RAM, ReRAM, *In-situ* TEM, Operation mechanism, Reliability

Resistive random access memories (ReRAMs) have great potential as a candidate for next-generation nonvolatile memories for the high speed, high density storage per cost [1] and their ability to the neural network devices. In order to analyze the reliability of ReRAMs and to find out the origin of the failures, it indispensable to understand the resistive switching mechanism. Since the transmission electron microscopy (TEM) provides a high resolution images of the nanostructure, *in-situ* TEM should be a powerful tool for the analysis. In our *in-situ* TEM system [2, 3], repeatable switching characteristics, are achieved together with clear images of formation and rupture of conductive filaments corresponding to the low and high resistance states.
In this work, we used several kinds of Cu-based ReRAM (CBRAM: Conductive Bridge RAM). TEM samples are fabricated by two methods. One is an ion-shadow method [4, 5], which is an ion milling technique with carbon mask particles. The other is FIB that is a conventional technique to make a sample observable in TEM. Almost the same characteristics as those measured at the outside of TEM by the use of real ReRAM cells are achieved in TEM by the both method. Fig. 1 shows an example of *I-V* switching characteristics of Cu-Te based ReRAM [6, 7] and the corresponding TEM images [2, 3]. It was clearly shown that a dark spot corresponding to a conductive filament appeared by SET and erased after RESET. These resistive switching characteristics by *I-V* sweep were reproducible at least 60 cycles in TEM. In addition, SET/RESET pulse operation more than 100k times are confirmed during TEM observation as shown in Fig. 2.
These results clearly indicate that the in-situ TEM will be a powerful tool to guarantee the reliability of ReRAMs.

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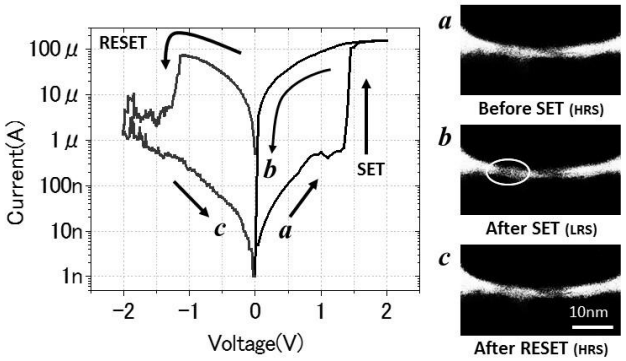

Fig. 1. I-V characteristics measured in TEM with current compliance of 150 μA, and TEM images just before SET, just after SET and just after RESET.

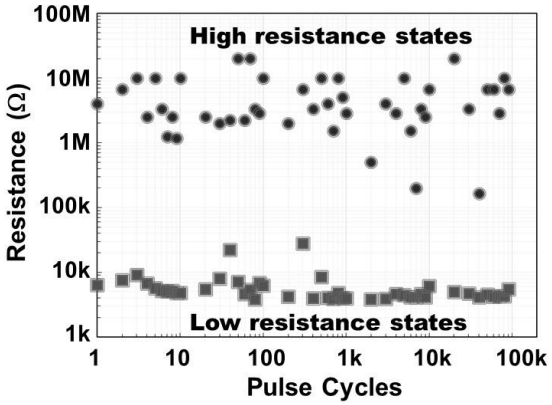

Fig. 2. SET/RESET pulse cycles measured in TEM.

STRAIN ENGINEERING FOR GeSn/SiGeSn MULTIPLE QUANTUM WELL LASER STRUCTURES

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Optically pumped GeSn laser have been realized, thus alloying of group IV elements germanium (Ge) and tin (Sn) has a large potential to be a solution for Si-photonics, since a direct bandgap for Sn incorporations above ~9 at.% is obtained [1]. The value of the bandgap can further be controlled by adding Si into the mix, which can be exploited for the formation of heterostructures for carrier confinement [2]. However, a sufficiently large difference in energy ΔE between the indirect L-valley and the direct Γ-valley is required to achieve room temperature lasing. Recently lasing was reported at 180K in GeSn alloys with Sn concentrations as high as 22,3% [3]. Alternatively ΔE can be increased by adding tensile strain to the GeSn layers. Here we will discuss that an appropriate combination of Sn concentration and strain will be advantageous to tailor gain and temperature stability of the structures.

Here, we will present a comprehensive characterization of direct bandgap heterostructures multiple quantum well (MQW) structures, formed from active GeSn layers and SiGeSn ternary claddings. Fig. 1 shows spectra of an optically pumped µ-disc MQW laser taken at various optical pump power. The data reveal a lasing threshold at 20 K from light in/light out curves of 39 kW/cm2, which is an order of magnitude smaller than the threshold observed for devices fabricated from bulk GeSn layers, clearly evidencing the superiority of MQW structures over bulk layers. The performance of the optically pumped laser were investigated in dependence of temperature, pump power and excitation wavelength. The gained insight reveals that carrier dynamics are crucial and that the “directness” of the bandgap $\Delta E=E_\Gamma-E_L$ is a decisive parameter on the path towards an electrically pumped laser operating at room temperature. Fig. 2 compares the modeled carrier distribution in MQW and heterostructures. The population in the Γ-valley reflects the maximum operation temperature of the laser. The impact of design, composition and strain of the SiGeSn/GeSn MQW structures on ΔE will be discussed.

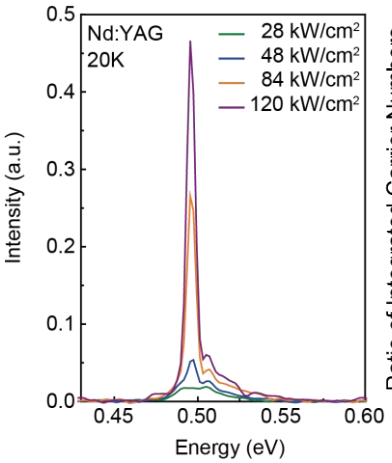

Fig 1: Power dependence of lasing spectra taken at 20K of a optically pumped GeSn/SiGeSn µ-disc laser. Threshold at 20 K from LL: 39 kW/cm^2

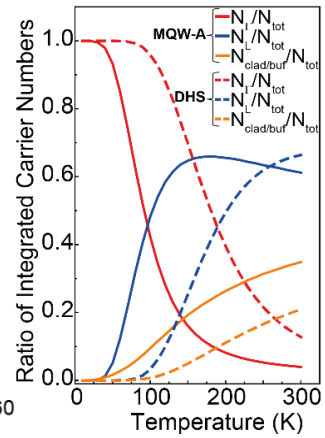

Fig 2: Modeled electron numbers in the Γ- (red) and, L-valleys (blue) and in the barriers layer (orange) as a fraction of total electron concentration, MQW (solid line) and DHS (dashed line).

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RELIABILITY DEGRADATION PHENOMENA IN OXIDE THIN FILM TRANSISTORS

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Key Words: Metal Oxide Thin Film, Thin Film Transistor, Reliability, Display, OLED

Oxide Thin Film Transistors have been extensively studied as driving elements for realizing next-generation displays. For this purpose, not only improvement of performance but also improvement of reliability are indispensable. Compared to amorphous Si and low temperature polycrystalline Si which have been put into practical use, unique deterioration phenomenon has been reported by various researchers. In this paper, we introduce the reliability of this oxide thin film transistor, mainly on degradation mechanism and improvement measures. First, we introduce deterioration phenomena against stress such as constant voltage application, AC voltage application, light irradiation, Joule heat and its mechanism. Next, we will also introduce the influence of hydrogen in the oxide material on the reliability of the device, measures for improving the passivation material and measures for improving the reliability of the device by improving the manufacturing process.

Fig.1 shows the change of the transfer characteristic due to AC stress. In the oxide TFT, a shift in the negative direction of the threshold value was observed by the gate pulse (Vg = ± 20 V). It was also accelerated with increasing frequency. As a result of changing the rising and falling time of the pulse, the deterioration depends on the fall time, and the sharper the threshold change is. We believe that degradation of hot carriers generated at the falling edge of the pulse is due to deterioration.

Figure 2 shows the Joule heating phenomenon when AC stress (Vg = Vd = ± 15 V) is applied to the oxide TFT. The maximum temperature during pulse application decreased with increasing frequency. The reason for this is believed to be that the electric field effectively applied to the TFT was relaxed.

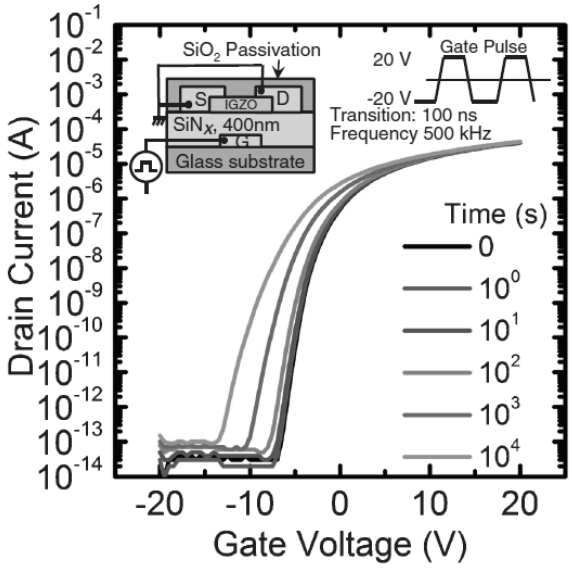

Fig.1 Degradation of a-IGZO by dynamic stress

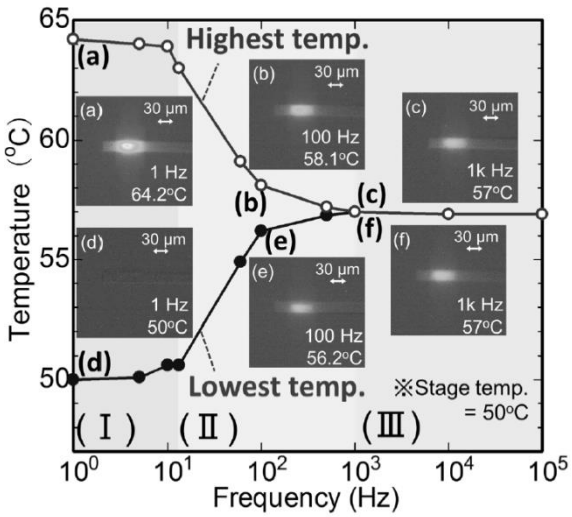

Fig.2 Frequency dependence of Joule heat in a-IGZO

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CARRIER TRANSPORT AND BIAS STRESS STABILITY OF IGZO TFT WITH HETEROJUNCTION CHANNEL

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Key Words: In–Ga–Zn–O (IGZO), Thin-Film Transistor (TFT), Heterojunction channel

An InGaZnOx (IGZO) thin-film transistor (TFT) has been received considerable attention for use in next-generation displays owing to their excellent electrical properties. Although a field effect mobility (m_{FE}) of the IGZO TFT (10~15 $cm^2V^{-1}s^{-1}$) is over ten times larger than that of an amorphous silicon TFT, further enhancement of the m_{FE} is desired to expand their applications. Several approaches have been proposed to improve the m_{FE} of oxide TFT. Among them, it is known in the IGZO material system that an increase of In content is effective to enhance the m_{FE} of the IGZO TFT since a conduction band of the IGZO is mainly composed of an In 5s orbitals. However, high In composition leads to an increase carrier concentration (oxygen vacancy) in the film, result in a degradation of TFT properties such as negative shift of threshold voltage and hump in transfer characteristics.
In this presentation, the TFT with a heterojunction IGZO channel was investigated to enhance m_{FE} and bias stress and temperature stability (PBTS). For the hetero-junction channel, a high-In composition IGZO layer (IGZO-high-In) was deposited on a typical compositions IGZO layer (IGZO-111) to form the type-Ⅱ energy band diagram which possess a conduction band discontinuity (ΔEc) of 0.39 eV as shown in Fig. 1(a). Thickness of the IGZO-high-In layer was varied at 2.5, 5.0, and 10 nm, while that of the IGZO-111 layer was maintained to 10 nm to keep the constant electric field in the hetero-junction interface when gate voltage (V_{GS}) was applied. Figure 1(b) shows the transfer characteristics of the hetero-IGZO TFTs with the IGZO-high-In thicknesses of 2.5, 5.0, and 10.0 nm. The hetero-IGZO TFT with a 2.5-nm-thick high-In on IGZO-111 showed a m_{FE} of 11.3 $cm^2V^{-1}s^{-1}$, which is almost the same value as the homogeneous IGZO-111 TFT. However, the m_{FE} of the hetero-IGZO TFT increased with an increase of the IGZO-high-In thickness deposited on IGZO-111. In particular, the m_{FE} of the hetero-IGZO TFT with a 10-nm-thick high-In back-channel exhibited 20.1 cm^2 $V^{-1}s^{-1}$ which was twice as high as conventional IGZO-111 TFT. To investigate the carrier transport mechanism in the hetero-IGZO TFTs, current densities in the IGZO channel were extracted by device simulation (ATLAS) as shown in Fig. 1(c). Since the ΔEc is formed at the hetero-junction interface, it acts as an energy barrier for electron confinement at the hetero-junction interface. At a gate voltage of below 10 V, a drain current mainly flowed at the high-In layer; resulting in the m_{FE} improvement. On the other hand, when the V_{GS} further increased to +20 V, the drain current flowed through both the front and hetero-junction interfaces. These results indicate that the changing of carrier transport pass, which depends on the applied V_{GS}, leads to the single peak of the m_{FE} of the hetero-IGZO TFTs as shown in Fig. 1(b). Detail carrier transport mechanism and their PBTS reliability of hetero-IGZO TFTs will be discussed at the conference.

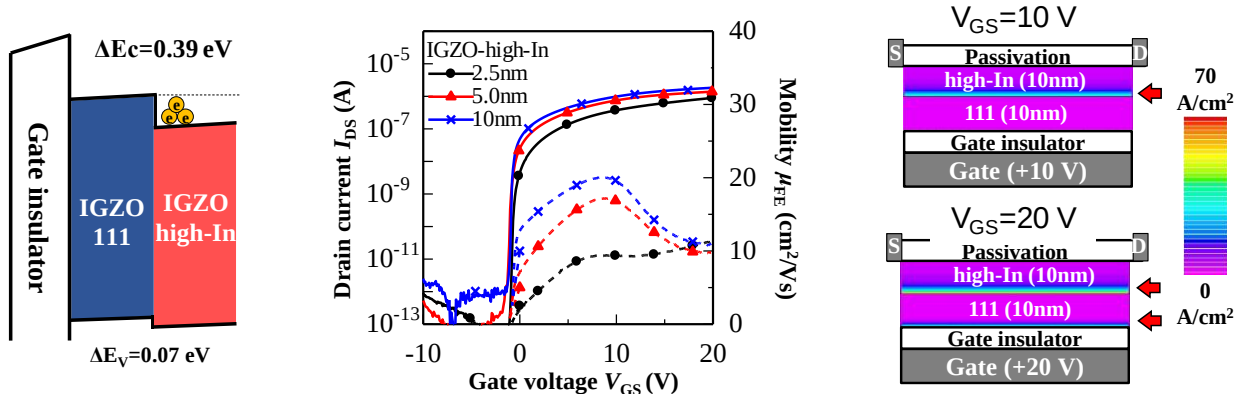

Figure 1 (a) Schematic illustration of energy band diagram, (b) transfer characteristics (experiments), and drain current density (extracted by device simulation) of the hetero-IGZO TFT

RELATIVELY LOW-TEMPERATURE PROCESSING AND ITS IMPACT ON DEVICE PERFORMANCE AND RELIABILITY

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Key Words: thin-film transistor, transistor, ZnO, IGZO, MoS_2.

Non-silicon, large-area/flexible electronics for the internet of things (IoT) has acquired substantial attention in recent years. Key electron devices to enable this technology include metal-oxide-semiconductor field effect transistors (MOSFETs), where ultra-thin and/or low-dimensional (i.e., 2D to a few layers) semiconductor materials may be required, like those found in thin-film transistors (TFTs) and transition metal dichalcogenide (TMD) FETs [1,2]. Whether TFT or TMDFET, a relatively low-temperature process commensurate with large-area/flex applications to enable large (i.e., greater than 300 mm) and/or flexible substrate fabrication is required. Furthermore, TMD materials may be implemented as the channel semiconductor to function as an ultra-thin body to mitigate short channel effects and extend further scaling as the future progresses in CMOS scaling. In addition, the gate dielectric insulator is another vital component of any MOSFET that requires investigation as part of the MOS stack in these types of transistors. Lastly, semiconductor materials mentioned herein do not have a universally accepted way to introduce dopants to form sources and drains. Thus, metal-semiconductor contacts are employed where the interface region of the contact plays a critical role in determining the conductivity/resistivity of the contact. Moreover, how the metal-semiconductor interface are formed also impacts the quality of the contact. Therefore, exploration of low-temperature processing, interfaces, and their impact on device performance and reliability will be critical to eventual implementation in future technologies. To ascertain the impact of low-temperature fabrication and critical interfaces, several process approaches and electrical characterization methods were employed [1-6]. In one case, for a TMD FET contact study, an oxygen plasma exposure in the contact region on MoS_2 (a TMD material) is done prior to titanium deposition. The results demonstrate that contaminants and photoresist residue that still reside after development can noticeably impact electrical performance (Fig. 1). The O_2 plasma removes the residue present at the surface of MoS_2 without the use of a high temperature anneal, and subsequently improves the device performance significantly (Fig. 1) [1]. In another case, for a MOS-based TFT study, an investigation of low-temperature (> 115°C) deposited zinc-based semiconductors was executed (Fig. 2). For ZnO and IGZO, saturation mobilities of 14.4 and 8.4 $cm^2/V\text{-}s$, along with threshold voltages of 2.2 V and 2.0 V were obtained, respectively, demonstrating robust devices that also have an on/off ratio > 10^8, with I_{OFF} lower than 10^{-12} A. Furthermore, a hot carrier stress methodology demonstrated threshold voltage (V_{TH}) shifts of 0.4 V and 1.8 V for ZnO and IGZO, respectively, after stress (Fig. 2) [2]. Continued research is required to ascertain the electrically active defects responsible for the V_{TH} shift.

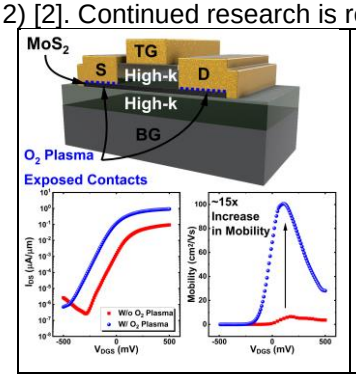

Fig. 1. MoS_2 TMD FET with and without an oxygen plasma treatment, where clear benefits are obtained from having the S/D contact regions exposed to an oxygen plasma prior to metal deposition.

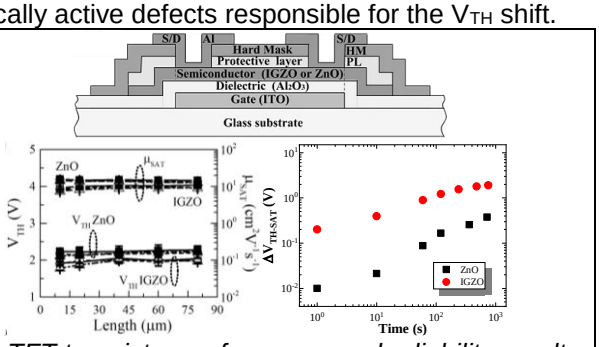

Fig. 2. TFT transistor performance and reliability results.

Acknowledgements: This work was supported in part by NSF CAREER Award ECCS-11139986, AFOSR project FA9550-18-1-0019, CONACYT and RD Research Technology USA, LLC.

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RELIABILITY OF FLEXIBLE LOW TEMPERATURE POLY-SILICON THIN FILM TRANSISTOR

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Key Words: Flexible LTPS TFT, Mechanical bending stress, Abnormal hump

This work reports the effect of mechanical stress-induced degradation in flexible low-temperature polycrystalline-silicon thin-film transistors. After 100,000 iterations of channel-width-direction mechanical compression at R=2mm, a significant shift of extracted threshold voltage and an abnormal hump at the subthreshold region were found. Simulation reveals that both the strongest mechanical stress and electrical field takes place at both sides of the channel edge, between the polycrystalline silicon and gate insulator. The gate insulator suffered from a serious mechanical stress and result in a defect generation in the gate insulator. The degradation of the threshold voltage shift and the abnormal hump can be ascribed to the electron trapping in these defects. In addition, this work introduced three methods to reduce the degradation cause by the mechanical stress, including the quality improvement of the gate insulator, organic trench structure and active layer with a wing structure.

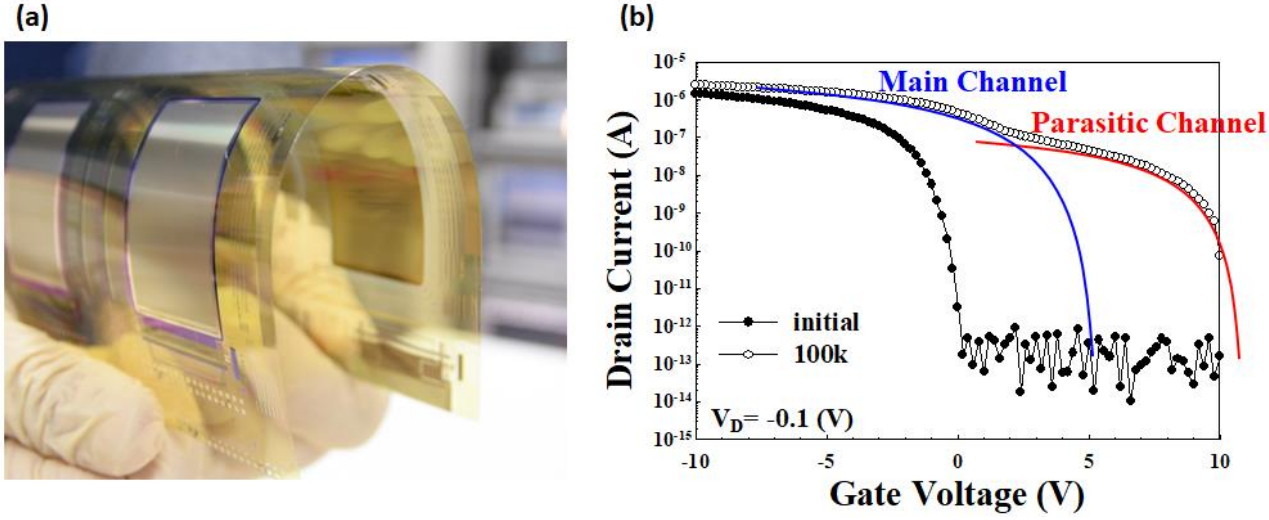

Figure 2 – (a)Photo of our flexible LTPS TFT. (b)I_D-V_G transfer characteristics with V_D=-0.1V for devices undergoing 100,000 iterations of width-axis compression bending.

CHALLENGE OF CRYSTALLINE IGZO CERAMICS TO SILICON LSI–ITS APPLICATION TO AI AND DISPLAYS

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Key Words: oxide semiconductor, ceramic matrix composites, IGZO

We found crystalline IGZO ceramics having a layered structure, a crystalline oxide semiconductor called *c*-axis-aligned crystalline In-Ga-Zn oxide (CAAC-IGZO) in 2009. Recent research has revealed that CAAC-IGZO exhibits a structure in a boundary region between amorphous and crystal structures [1]. We are convinced that CAAC-IGZO is a novel crystalline phase, as shown in Table 1.

A field effect transistor (FET) using the crystalline IGZO ceramics with L/W = 0.8μm/100mm exhibits an off leakage current of 6yA/μm (10^{-24}A/μm) at 85°C, which is such a low current that FETs using Si, the dominant semiconductor material, cannot ever achieve [2]. In the display industry, FETs utilizing this feature have been increasingly mounted on panel backplanes and widely adopted in various products such as TVs and smartphones. CAAC-IGZO FETs have a high on/off ratio and thus are being applied also to the field of LSI; a 60nm-node prototype line for mass production started operating [3]. CAAC-IGZO FETs are effective for applications such as FPGA, GPU, and DRAM, and are now being developed to target image processors and artificial intelligence (AI).
CAAC-IGZO FETs are known to have mobility that does not deteriorate at high temperatures [5]. Figure 1 shows cutoff frequency (f_T) of a CAAC-IGZO FET and a Si FET at varying temperatures. While there is a difference in f_T of the Si FET between 27°C and 150°C, a change in f_T between different temperature conditions is small in the CAAC-IGZO FET. Moreover, f_T of the CAAC-IGZO FET is 33GHz, which is approximately 1/4 that of the Si FET (137GHz). These results demonstrate that the on-state current and field-effect mobility of the CAAC-IGZO FET do not decrease with increasing temperature.
As above, CAAC-IGZO FETs have a high on/off current ratio at high temperatures as well as at room temperature. Thus, circuits with the FETs enable standby power reduction, which is impossible for CMOS to achieve.

In the presentation, I will report electrical characteristics of the crystalline IGZO ceramics and provide its application examples in the display field and the possibility of application to the LSI area.

Table 3 – Classification of crystalline IGZO ceramics

Amorphous [5]	Novel boundary region: Crystalline [6]	Crystal [7]
completely amorphous	・ CAAC ・ nc ・ CAC excluding single crystal and poly crystal	・ single crystal ・ poly crystal

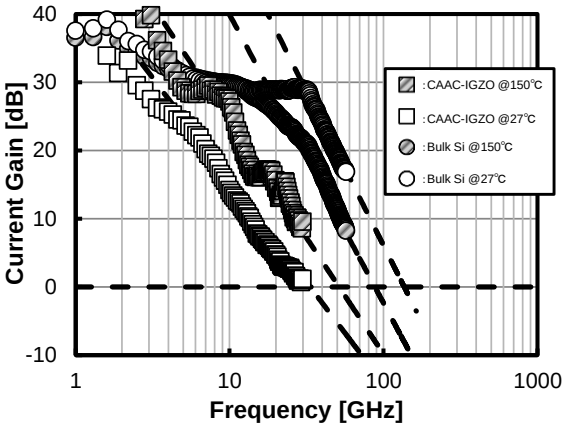

Figure 1 – Cutoff frequency (f_T) of CAAC-IGZO FET and Si FET at varying temperatures

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INTRODUCING NOVEL FUNCTIONAL MATERIALS AND LIQUIDS FOR BREAKING THE LIMIT OF MEMORY DEVICES

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Key Words: memory device, CBRAM, ionic liquid, MOF.

Memory devices with higher performance and higher density are being required to deal with drastically increasing data. However, we are, now, facing the limit of further improvement of memory performance. Related to this, semiconductor technology is facing a miniaturization limit and further increase in the density of memory devices is getting harder and harder. To overcome these issues, introducing novel materials that have unique physical and chemical properties that materials used in conventional silicon technology cannot provide into CMOS process is examined. For example, we hypothesized that the addition of ionic liquids (ILs) to conducting-bridge random access memory (CBRAM) would improve a cycling endurance as well as the switching voltages and data retention of CBRAM [1, 2]. Here, CBRAM has a simple structure of top electrode (TE)/metal oxide (MO)/bottom electrode, in which electrochemically active metals, such as Cu and Ag, are used as one of the two electrodes, which is defined as a TE in this study, and works as a memory device by the connection and disconnection of a CB consisting of the active metal that is eluted electrochemically from the TE. Our hypothesis was based on the expectation that the segregation of the eluted TE metal, which makes the CB too thick to be disconnected again and is a main factor causing a reset failure, could be avoided with the help of high ability of ionic liquids to enhance ionization and diffusion of the TE metal. We actually confirmed that switching voltages and their dispersions decreased by addition of metal containing ILs that were designed for the use in CBRAM. Another example is introducing metal organic frameworks (MOFs) into electric devices. MOFs inherently have periodically and densely aligned nano-scale pores due to self-assembled phenomena. We propose replacing a metal oxide film in CBRAM cell that works as a memory layer with MOF. This is because we expected that the nano-scale pores of MOF enhance ionic diffusion and the directionality of the diffusion along the pores, leading to superior performance including the improvement of the deviations of switching voltages and resistance. We developed a method that enables a selective synthesis of MOF crystal accurately at desired points. Combining the method with conventional microfabrication technic that is familiar with silicon process, CBRAM cells with the diameter less than 100 nm that contain a single MOF crystal each as a memory layer could be fabricated successfully. We observed resistive switching phenomena in theses CBRAM cells, meaning that a single MOF crystal works as CBRAM was achieved as a microfabricated electric device, for the first time. Our examples suggest that introducing novel functional materials and liquids such as MOFs and ionic liquids into electric devices is effective in overcoming the limit of improvement of performances including further miniaturization.
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FLEXIBLE ORGANIC THIN FILM TRANSISTORS FOR HIGH-PERFORMANCE BIOSENSORS

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Key Words: Organic Thin Film Transistor; Biosensor.

Solution-gated transistors have shown promising applications in biosensors due to the high sensitivity, low working voltage and the simple design of the devices. Solution-gated transistors normal have no gate dielectric and the gate voltages are applied directly on the solid/electrolyte interfaces or electric double layers near the channel and the gate, which lead to very low working voltages (about 1 V) of the transistors. On the other hand, the devices can be easily prepared by solution process or other convenient methods because of the much simpler device structure compared with that of a conventional field effect transistor with several layers. Many biosensors can be developed based on the detection of potential changes across solid/electrolyte interfaces induced by electrochemical reactions or interactions. The devices normally can show high sensitivity due to the inherent amplification function of the transistors. In this talk, I will introduce several types of biosensors studied by our group recently, including DNA[1], glucose[2], dopamine, uric acid[3], cell[4], protein [5] and bacteria sensors, based on flexible solution-gated organic thin film transistors. The biosensors show high sensitivity and selectivity when the devices are modified with functional nano-materials (e.g. graphene, Pt nanoparticles) and biomaterials (e.g. enzyme, antibody, DNA) on the gate electrodes or the channel. Furthermore, the devices are miniaturized successfully for the applications as sensing arrays [6]. The solution-gated organic devices are also used for voltage-controlled drug release in aqueous solutions [7]. It is expected that the solution-gated organic transistors will find more important applications especially wearable electronics for healthcare in the future [8,9].

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MECHANICAL BALL SHEAR, ELECTROMIGRATION AND THERMAL CYCLING RELIABILITY TESTING ON NOVEL SOLDER INTERCONNECTS OF HIGHLY INTEGRATED CHIPS FOR ADVANCED APPLICATIONS

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Key Words: Pb-free solder; Thermal cycling; Ball shear; Electromigration;

In the near future, Ultra Large Scale Integrated Circuits (ULSI) with high integration has drawn the huge attention because of its potential applications in VR, AI, IoTs and automotive regions. Thermal budget and reliability concerns are two major issues that are urgently needed to be solved for these technologies. Since the increasing integration of ICs might lead to low yield concern, low fabrication temperature is expected to reduce the thermal impact on ICs properties. Besides, better reliability is also required to the electric devices for those to work under harsh outdoor environments. This study is tended to be focused on the novel solder bonds for the advanced ICs, including low temperature solder, Cu-core solder ball, and their response under various reliability tests. Three main reliability tests: (1) ball shear test, (2) electromigration test (EM) and (3) thermal cycling test (TCT), are conducted to evaluate the reliability of solder bonds. In this work, the novel Bi-40In solder alloy with improved mechanical property and the EM-resisted Cu-core solder ball are demonstrated. The re-designed low temperature solder joint reveals the superior ball shear strength than that of conventional eutectic Bi-33In joint. Additionally, the interconnects using Cu-core solder ball show the high resistance against EM under current stressing. Regarding TCT, the assemble joints with various grain structures are tested to realize the effects of Sn grain size on joint degradation and the possible ways for relieving the thermomechanical stress caused by TCT. The microstructure, elemental characteristics and grain structure are analyzed by FE-SEM, FE-EPMA and EBSD, respectively. The failure mechanisms for all reliability tests are addressed and discussed in details as well.

NON-VOLATILE n^+-TiO_2 CHANNEL FETs WITH FERROELECTRIC HfO_2

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Key words: ferroelectric, HfO_2, TiO_2, junctionless

Ferroelectric FETs (Fe-FETs) have been investigated for many years, because it may offer versatile opportunities in terms of low-power nonvolatile FETs. Recently, ferroelectric HfO_2 was found experimentally [1], and has been investigated for various promising applications, because HfO_2 is now dominantly used for advanced CMOS gate stacks. Substantial challenges of ferroelectric FETs for advanced device design are how to control the interface with semiconductors as well as the ferroelectric material properties. Furthermore, since the polarization charges are always too high for conventional semiconductor channels, it is required to reconsider the semiconductor material as well as appropriate FET structure. This paper discusses opportunities of ferroelectric FETs using doped HfO_2 on an oxide semiconductor channel, and demonstrates its nonvolatile FET performance.

We paid attention to ferroelectric N-doped HfO_2 [2], because very small N was needed to make HfO_2 ferroelectric and N may not degrade the interface as compared with metallic cation as the dopant. N-doped HfO_2 films were grown by rf-sputtering by introducing controlled amount of N_2 into Ar, flowed by PDA at 600°C. 40-nm-thick HfO_2 exhibited typical P-E characteristic. Although Si is practically the best material for the channel material, when a huge polarization charges (10~100 μC/cm^2) in common ferroelectric films, including HfO_2, are taken account, high permittivity channel materials would be better. Thus, high mobility (~10 cm^2/Vsec, k~100) TiO_2 grown by PLD [3] was employed as the channel material. Furthermore, since charge accumulation type FETs were considered to be inevitably affected by the interface quality, the junctionless type FET was designed. Fig. 1 (a) shows a schematic view of 40-nm-thick 0.34% N-doped HfO_2 film with 10-nm-thick 0.2 wt.% Nb-doped TiO_2 as the n^+-type channel layer, and (b) shows the top view under the microscope. FET characteristics are shown in Fig. 2, in which (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} characteristics are shown. The saturation behavior is a little degraded in I_{DS}-V_{DS}, while the subthreshold characteristics show the counter-clockwise hysteresis and the surprisingly low off-leakage current. The hysteresis width is roughly 5 V in this case, because the coercive field of HfO_2 is rather large. This value is adjustable by changing HfO_2 thickness. An appropriate electrode material selection in place of Al is needed to adjust V_{th}. Ferroelectric HfO_2 scalability and reliability have been already investigated in capacitors, and the remanent polarization gradually increased with the HfO_2 thickness decrease down to 5 nm. Furthermore, thin ferroelectric HfO_2 (~5 nm) had a higher cycling tolerance than thick (30 nm) one [4]. Therefore, both scalability and reliability in thin ferroelectric HfO_2 FETs are very promising for versatile applications of scaled devices as well as for back-end non-volatile switches.

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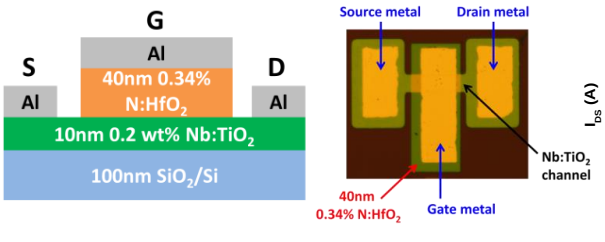

Figure 1 Schematic view of Fe-FET with ferroelectric N-doped HfO_2 (40 nm) on Nb-doped TiO_2 (10 nm). This is the junctionless type FET. (b) Top view of the present FET. Electrode material is Al for source, drain and gate.

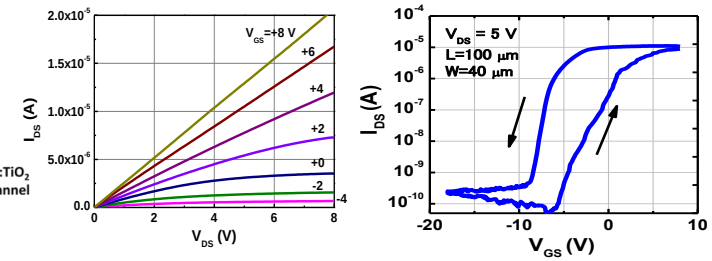

Figure 2 (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} characteristics in N-doped HfO_2 on Nb-doped TiO_2 channel. V_{th} is not optimized in this device, but a very stable memory window is exhibited.

LANGMUIR-TYPE MECHANISM FOR IN-SITU DOPING IN CVD SILICON AND GERMANIUM EPITAXIAL GROWTH

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Key Words: Langmuir, In-situ doping, CVD, Si, Ge

High performance Si-based devices require atomically ordered interface of heterostructures and doping profiles as well as strain engineering due to the introduction of Ge into Si. The fabrication of atomic-level steep doping profiles needs the suppression of dopant segregation during epitaxial growth [1]. In this work, in-site doping of P and B in CVD Si, Ge and $Si_{1-x}Ge_x$ epitaxial growth using SiH_4-GeH_4-dopant (PH_3 and B_2H_6)-H_2-He gas mixtures [1, – 7] is reviewed based on the Langmuir-type surface adsorption and reaction scheme.
Anomalous heavy doping of P is explained, assuming that GeH_4 adsorbs/reacts partially at the sites where PH_3 molecules have been adsorbed on (100) surface, although the sites become inactive for both the SiH_4 and GeH_4 adsorption/reactions on the surface [2]. Based on the experimental results that P atoms of 3, 2, 1 atomic layer is formed self-limitedly on the Si-Si, Si-Ge, Ge-Ge sites by PH_3 at the epitaxial growth temperature [2 – 4], the adsorption/reaction site density for PH_3 at each site is assumed. The adsorption and desorption rate constants of PH_3 and the incorporation rate constant of P atoms into the epitaxial layer from the adsorbed PH_3 molecules at each site are obtained numerically by fitting the experimental data for low PH_3 partial pressure region to the modified Langmuir-type mechanism. The segregation coefficient between surface coverage of PH_3 molecules and the concentration of P incorporated into the grown film at each site and growth rate constant of GeH_4 on adsorbed PH_3 molecules are also obtained numerically from the data for high PH_3 partial pressure region. The adsorption rate constant of SiH_4 and GeH_4 and reaction rate constant of SiH_4 at each site in refs. 2 are used.
Anomalous heavy doping of B is explained, assuming that SiH_4, GeH_4 and B_2H_6 adsorb/react partially at the sites where B_2H_6 molecules have been adsorbed on (100) surface [5]. It was confirmed that B atoms deposit continuously without self-limitation at the $Si_{1-x}Ge_x$ epitaxial growth temperature [6] and B atoms enhances the SiH_4 adsorption/reaction [7]. Therefore, it is also assumed that there is no segregation of B on the grown surface.
From these results, fairly good agreement is obtained between experimental data and the modified Langmuir-type mechanism for P doping as shown in Fig. 1 and for B doping.
These results demonstrate the capability of CVD for atomic level steep doping in Si, Ge, $Si_{1-x}Ge_x$ epitaxial growth in ultra large scale integration.
The author wishes the co-authors of the following references for encouragement and stimulating discussion in executing this study and his thanks to staffs, students for contributions for the research works at Tohoku University.

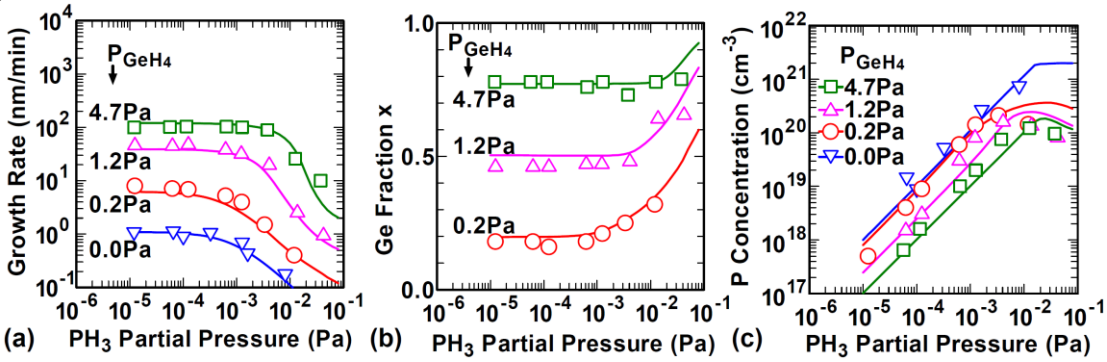

Figure 1 – Dependences of (a) growth rate, (b) Ge fraction, and (c) P concentration on the PH_3 partial pressure for epitaxial $Si_{1-x}Ge_x$ film formed at 550°C in a SiH_4-GeH_4-PH_3-H_2 gas mixture. The total pressure and the SiH_4 partial pressure are 30 Pa and 6.0 Pa, respectively. The solid lines are calculated from the fitting parameters based on the modified Langmuir-type mechanism.

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GERMANIUM-TIN SEMICONDUCTORS: A VERSATILE SILICON-COMPATIBLE PLATFORM

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Key Words: Silicon/Germanium, Germanium-tin, Direct bandgap, Integrated photonics, Quantum wells, Nanowires

Compound semiconductor alloys have been successfully used for a precise and simultaneous control of lattice parameters and bandgap structures bringing to existence a variety of functional heterostructures and low-dimensional systems. Extending this paradigm to group IV semiconductors will be a true breakthrough that will pave the way to creating an entirely new class of silicon-compatible ultra-fast/low-power electronic, optoelectronic, and photonic devices. With this perspective, germanium-tin ($Ge_{1-x}Sn_x$) and germanium-silicon-tin ($Ge_{1-x-y}Si_xSn_y$) alloys have recently been the subject of extensive investigations as new material systems to independently engineer lattice parameter and bandgap energy and directness. The ability to incorporate Sn atoms into silicon and germanium at concentrations about one order of magnitude higher than the equilibrium solubility is at the core of these emerging potential technologies. In this presentation, we will address the epitaxial growth and stability of these metastable semiconductors. We will also discuss the optical and electronic properties as well as the nature of the atomic order in Sn-rich group IV semiconductors. We will show that lattice strain engineering is critical to facilitate the incorporation of Sn at concentrations reaching, for in stance, nearly 20at.% in GeSn while suppressing Sn surface segregation and composition gradient. The basic properties of these GeSn layers will be discussed in the light of extensive optical and microscopic investigations. Moreover, we will also demonstrate that GeSn can be effectively used as a template to grow highly tensile strained Ge quantum wells. Results of the investigations of electronic properties of these new family of low-dimensional systems will be discussed. This includes the effects on strain level and nature (compressive vs. tensile) on charge carriers confinement and mobility. Finally, new concepts involving Ge/GeSn core-shell nanowires will be presented and their potential as versatile building blocks for electronics, integrated photonics, and quantum information will be addressed.

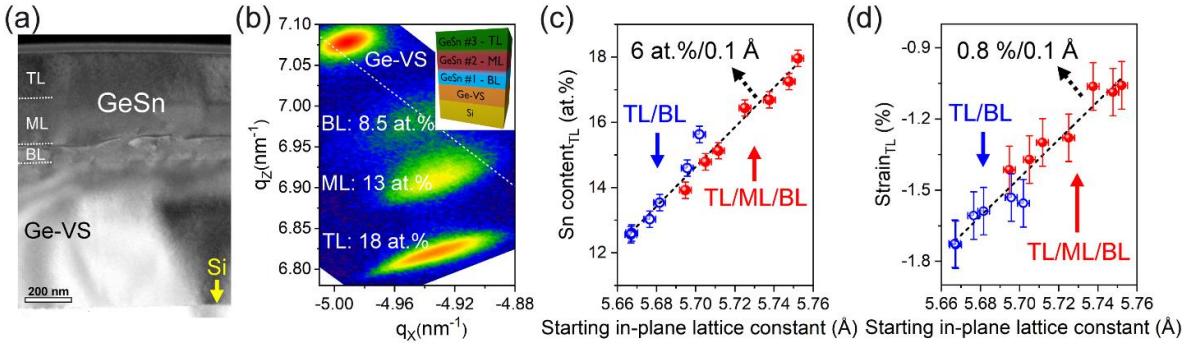

Figure 4 – GeSn top-layer/middle-layer/bottom-layer (TL/ML/BL) stack grown on a Ge virtual substrate. (a) TEM image. (b) XRD reciprocal space map. (c), (d) Effect of starting in-plane lattice constant on Sn incorporation and residual strain in the top layer.

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HIGH PERFORMANCE GAS SENSOR PLATFORM BASED ON INTEGRATED SENSING MECHANISMS

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Key Words: Gas sensor platform, resistive-type, TFT-type, FET-type, ZnO

We introduce a gas sensor platform consisting of resistive sensor, thin film transistor (TFT) type sensor, and Si-based field effect transistor (FET) type sensor fabricated on the same wafer. The FET type sensor has a horizontal floating gate interdigitated with the control gate. The schematic structures of these gas sensors are shown in Fig. 1. These gas sensors can be fabricated using only 5 masks. The sensing layer of these sensors is a 15nm thick *n*-type ZnO film prepared using atomic layer deposition (ALD) in the final process step. Although these sensors have the same sensing material, they have different sensing characteristics because of different sensing mechanisms. Our group has reported the studies of resistive- and FET-type gas sensors having ALD ZnO sensing layer previously [1], [2]. Fig. 2 shows the transfer (*I-V)* characteristics of these sensors. These sensors have different sensing characteristics when exposed to 500 ppb of oxidizing gas, NO_2. When exposed to NO_2 gas, the currents of resistive- and TFT-type gas sensors are decreased [2]. On the other hand, the drain current of the FET-type gas sensor increases when exposed to NO_2 gas [1], [2]. As a result, the difference in response of these sensors can be used as a fingerprint to more accurately detect the target gas in the gas sensor platform composed of three types of gas sensors.

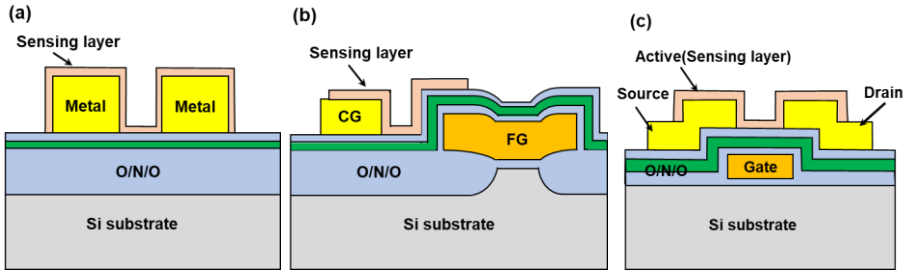

Figure 5 Cross-sectional schematic views of the (a) resistive-, (b) FET-, (c) TFT-type gas sensors.

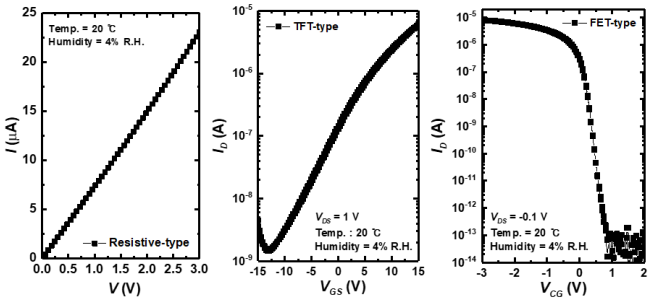

Figure 2 Transfer (I-V) characteristics of the (a) resistive-, (b) nTFT-, (c) pFET-type gas sensors.

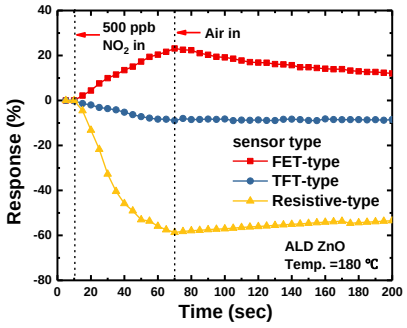

Figure 3 Gas response of the three-types of the sensors to 500 ppb NO_2 gas at 180℃. Here drain biases (V_{DS}) of the nTFT- and pFET-type sensors are 1 V and -0.1 V, respectively.

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EMBEDDED DRAM USING C-AXIS-ALIGNED CRYSTALLINE In-Ga-Zn OXIDE FET WITH 1.8 V-POWER-SUPPLY VOLTAGE

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Key Words: Oxide Semiconductor, CAAC-IGZO, ULSI, DRAM, Low Power.

An embedded memory using c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO) FETs with an extremely low off-state current on the order of yoctoamperes (yA) (yocto- is a metric prefix denoting a factor of 10-24) is known as a potential next-generation memory [1][2]. A dynamic oxide semiconductor RAM (DOSRAM), where each memory cell is composed of one CAAC-IGZO FET and one capacitor, enables long data retention and long interval of refresh operations with an advantage of extremely low off-state current of the CAAC-IGZO FET. However, negative backgate voltage (Vbg) and word-line driving voltages of 0/3.3 V (VSSL/VDDH) had been required for an access transistor of the memory cell to satisfy high on-state current and low off-state current. This work shows that DOSRAM operates with 1.8 V-power supply voltage by using a novel driving method. Figure 1 shows Vg-Id performance of a CAAC-IGZO FET used as a cell transistor. The threshold voltage (Vth) of the CAAC-IGZO FET is controlled by changing a level of Vbg, whereas Vth of the Si FET is controlled by channel doping. Figure 2 shows a block diagram of a prototyped DOSRAM. The refresh rate in DOSRAM mainly depends on the leakage current of cell transistors. To reduce the refresh rate to once an hour, the off-state current of the cell transistors on a non-selected word line needs to be reduced to 200 zeptoamperes (zA) per FET (zepto- is a metric prefix denoting a factor of 10-21) or lower at 85□C. The required Vbg is -7.0 V to achieve such an off-state current at Vg □ 0 V, for example. To obtain approx. 100 MHz-driving frequency, the required on-state current is at least several microamperes. The voltage level difference in the word line, VDDH □ VSSL, is a factor that determines the on-state current, and in this work is fixed to 3.3 V so that the combination of Vbg and the word line voltage is optimized. The application of negative voltage to the word line enables the leakage current of the cell transistor to be maintained low even when Vbg is increased. For example, whereas the existing driving method meets the above off-state current value with Vbg □ -7.0 V and the VSSL □ 0 V, the novel driving method meets the value with Vbg □ 0 V and VSSL □ -1.5 V. In the novel driving method, VDDH □ 1.8 V. There has been a report of a reduction in leakage current of a memory cell by application of negative voltage to a top gate in DRAM using Si CMOS [3]. In contrast to it, DOSRAM including CAAC-IGZO FETs with L □ 60 nm has a leakage current of 200 zA or lower, which is 7-digit lower than that of the DRAM using Si CMOS, and enables longer data retention.

The evaluation results of the prototyped DOSRAM verify that a reduction in power-supply voltage from 3.3 V to 1.8 V is possible in terms of operation and data retention. This suggests a highly compatible and efficient configuration of an embedded DRAM and a logic circuit where signals can be transmitted with low VDD.

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A NEW DESIGN METHODOLOGY OF HIGHLY RELIABLE TFT BASED INTEGRATED CIRUCITS IN DISPLAY APPLICATIONS

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Key Words: design methodology, TFT based integrated circuits, high reliability, evolutionary aging.

Thin-film transistors (TFTs) technology is currently the dominant technology for pixel switching in display application. The new consumer electronics requires higher resolution and brightness, lower power consumption, multi-functional with new features such as flexible and foldable display. This drives TFT devices to deliver more complex functions. Owing to a sustained, enormous effort in TFT research and development and a continuous capital investment from the display industry around the world for the past three decades, the performance of TFT has not only surpassed the display requirements in most areas, but also go beyond the simply switch to more complex digital and analogue integrated circuits, for example, the flexible and narrow bezel displays integrated row drivers with TFT technology next to the pixel array. Such integrated circuits comprise thousands of switches operating together, requires an accurate analysis during design.

In the recent years, new display technologies, such as organic light-emitting diode (OLED) display and light-emitting diode (LED) displays have been emerging and become commercial reality due to certain advantages like self-luminous, high contrast, and etc. However, the OLED device has relative shorted lifetime and the current driving TFTs typically suffer from the electrical instability issue under high temperature and long-time stress condition. Thus, the reliability concerns in display have generated a considerable number of experimental studies and require careful analysis for the design of its pixel and integrated drivers. Particularly, individual TFTs are exposed to various stress condition in display operation with different degradation such as threshold voltage shift (ΔV_{th}) or mobility (μ) decreasing result in a failure of display operation, given that the performance of an aging TFT might deviate from expectation of original design, and moreover, it might influence its neighboring TFTs. Traditional design method considering device performance variation and device-level aging approach of ΔV_{th} and μ may not appropriate given that the traditional design of display pixel and driver circuit did not consider the evolutionary effects to each TFTs and different aging rate under various stress condition.

We proposed a design methodology for highly reliable display circuits with considering the dynamic time evolutionary degradation of TFT and OLED devices. The proposed methodology addresses the devices degradation issues from the circuit-level rather than device-level during the design, which improve the accuracy of the analysis for the stress pattern and the operating conditions on each individual device in the circuit. The proposed method could also be used for the lifetime prediction during the design, which could be great useful toward developing robust TFT-based circuits.

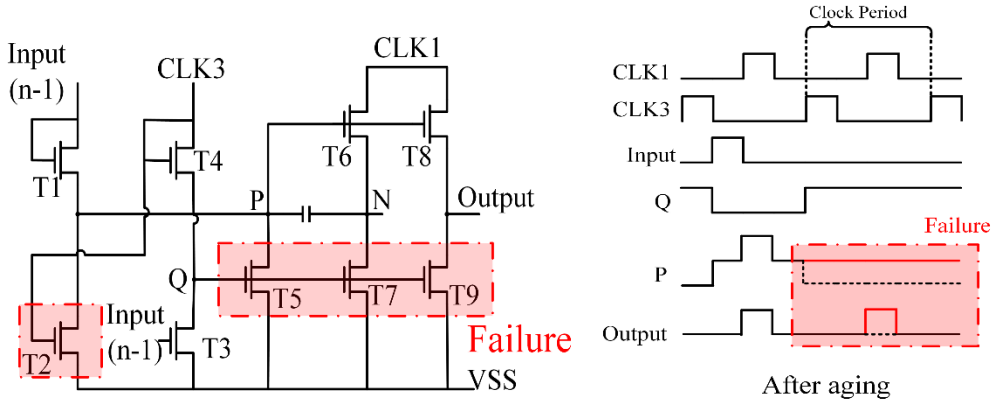

Figure 6 – The schematic diagram and timing of the scan driver with aging phenomenon

DUAL GATE LTPS TFT VERSUS OXIDE TFT

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There is of increasing interest for dual gate, dual sweep driving for TFTs to have higher drain current. We studied the dual gate structure of a-IGZO TFT by dual sweep, exhibiting much higher drain currents and better threshold voltage and smaller subthreshold swing. In this work we studied the dual gate LTPS TFTs and found very different results. The increase in drain current of LTPS TFT is found but the threshold voltage and SS are similar to those of a single gate TFT.

FABRICATION AND AC PERFORMANCE OF FLEXIBLE INDIUM-GALLIUM-ZINC-OXIDE THIN-FILM TRANSISTORS

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Key Words: Flexible electronics, Thin-film transistors, InGaZnO, Transit frequency, Scaling.

Flexible and conformable devices operated in contact with the human body, or fabricated using cost effective roll-to-roll techniques are one of the next major steps in the development of consumer electronics. Specifically, flexible transistors promise to enable new applications including rollable display backplanes or active RFID tags. Additionally, analog circuits such as amplifiers, buffers, or transceivers made from flexible transistors can be used to realize front-end conditioning and readout circuits for wearable sensors. Thin-film transistors (TFTs), fabricated on polymer substrates using oxide semiconductors, especially amorphous Indium-Gallium-Zinc-Oxide (IGZO), are particularly suitable to fabricate active electronics when bendability and electrical performance is required simultaneously. The IGZO TFTs presented here are manufactured on free standing polyimide foils using a maximum process temperature of 150°C. These TFTs are based on high-k Al_2O_3 insulating layers (deposited by Atomic Layer Deposition), metallic contacts, and RF sputtered IGZO. They exhibit state of the art performance including a field effect mobility of ≈15 cm^2/Vs, a threshold voltage of ≈0.3 V, an on-off current ratio $>10^8$, and a subthreshold swing of ≈125 mV/dec. They also stay fully functional while bent to tensile or compressive radii as small as 3.5 mm. However, while the DC performance of such IGZO TFTs is well understood, their AC performance has to be further investigated. Here, different approaches to improve their high frequency performance are presented and discussed. All devices are designed with ground-signal-ground contact pads to enable a reliable AC characterization using a two port network analyser. The measurements show that conventional bottom-gate TFTs, with a channel length of 3 µm, and gate overlaps of 15 µm allow a transit frequency up to 10.5 MHz. This value, which is in good agreement with the corresponding transconductance and gate capacitance measurements, is limited by parasitic resistances and capacities as well as by the lateral TFT dimensions. These limitations is caused by the difficulty in reliably realizing small features on free standing polymer substrates, due to thermal expansion. To improve the maximum operation frequency, different methods to reduce the TFT channel length have been developed. As shown in Figure 1, these include flexible TFTs defined by self-alignment, focused ion beam (FIB), and direct laser writing (DLW), as well as vertical TFT structures. All devices are functional and exhibit channel length down to 160 nm. It was found that although traditionally smaller feature structures are beneficial, a careful optimisation of the gate capacitance, overlap capacitance, and contact resistance is required for flexible IGZO TFTs. Consequently, the shortest transistors do not exhibit the highest frequencies, but a record high transit frequency of 135 MHz, and exceptional maximum oscillation frequencies of 398 MHz are demonstrated for 500 nm long self-aligned flexible transistors. This is also validated by, a mathematical model to predict the AC performance of heavily scaled IGZO TFTs realized using different fabrication techniques. Finally, optimized TFTs can be used to realize entirely flexible analog circuits leading towards imperceptible electronic systems.

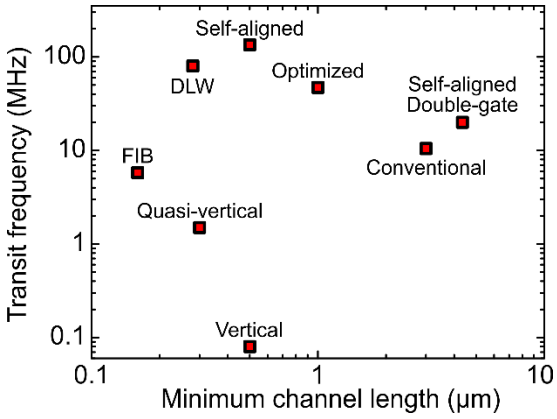

Figure 7 – Impact of different fabrication approaches on the geometry and measured AC performance of flexible short channel IGZO TFTs.

OBSERVATION OF THE BEHAVIOR OF ADDITIVES IN COPPER ELECTROPLATING USING A MICROFLUIDIC DEVICE

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Key Words: Damascene Process, Through Silicon Via, Suppressor, Accelerator, Leveler.

Nowadays, high performance of integrated circuits is owing its interconnections and packaging technologies, and copper electroplating is widely used for the fabrication of wirings since 1997, so called "The IBM shock". IBM announced chips with copper interconnects in 1997. The copper wirings were made by filling copper into vias in an insulating layer. Surprisingly, wet electroplating in acid copper sulfate was employed for the copper filling because preferential deposition from via bottoms, i.e. superfilling, was available by addition of several organic additives into the copper sulfate bath. However, at that time, the mechanism of superfilling was not clarified. Then, CEAC (Curvature Enhanced Accelerator Coverage) mechanism was proposed by Moffat et al. and the accelerator based theory is widely recognized as the principle of the superfilling for the sub-micron scale vias.

Recently, there are also many challenges in much larger scale copper wiring, such as TSV (Through Silicon Via). TSVs have the holes with quite high aspect ratio whose diameter is around 10μm and the deep holes are filled with copper by electroplating. Though the bottom-up superfilling is obtained, filling mechanism is not understood yet. Different form sub-micron scale filling, suppression behavior of additive is considered as an essential factor for the bottom-up filling as shown in figure 1. But critical suppression behavior is not well observed by conventional electrochemical measurements. Desorption of suppressing additive from plating surface seems to have important role, because Xis most limited. In this study, we made a microfluidic device to realize precise mass transport and quick switching of plating solutions, and in-situ observation of plating surface was performed.

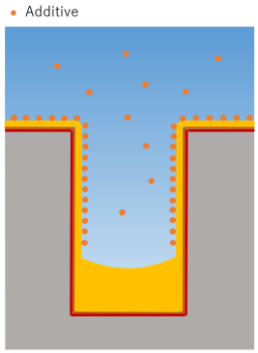

Figure 8- Additive inhibits deposition from top.

Figure 2 shows a result with a commercial leveler. Initially, VMS (virgin make-up solution) with no additive was supplied into the micro channel, and copper plating was performed on Pt working electrode with 100 μm in diameter. Then, the solution containing an additive was supplied. Finally, the solution was switched to VMS again and additive deactivation was monitored. With small overpotential (-550 mV vs. MSE), plating surface was covered by the additive and strong suppression was observed. After the plating solution was switched to VMS with no additives, localized depositions were observed all over the plating surface. While with large overpotential (-600 mV vs. MSE), strong suppression was observed only on up-stream region of the plating surface where bright smooth surface was kept during the leveler supply. After the solution change, suppression breakdown with localized depositions were observed gradually from the lower-stream region. Identical experimental procedure was applied to several additives and the behaviors were compared.

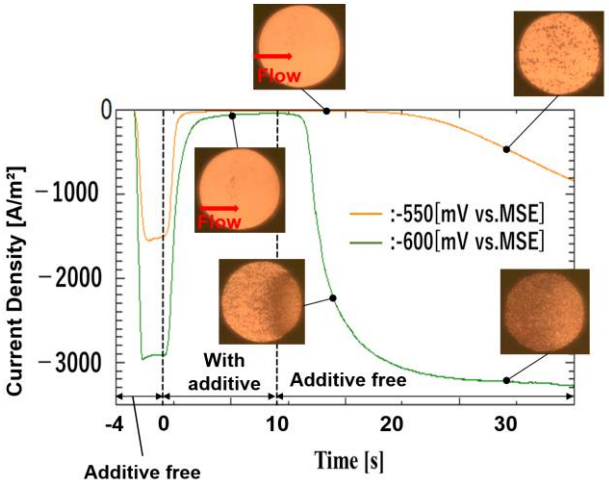

Figure 2- Additive supply was interrupted and in-situ observation of plating surface was carried out.

THERMAL OXIDATION KINETICS OF GERMANIUM

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Key Words: germanium, thermal oxidation, gate stack.

We have studied Ge gate stacks for many years, and demonstrated very interesting properties in Ge [1]. Recently we have published a review paper on Ge from viewpoints of device and process for CMOS applications. Through this study, we have noticed that GeO_2/Ge is so different from SiO_2/Si. It means that the oxidation kinetics of Ge should be studied carefully and understood correctly, though that of Si is almost understood.

We carried out the oxygen isotope (^{18}O) tracing experiments in Ge oxidation process. Figure 1 shows a comparison between Si oxidation and Ge one, inspected by the SIMS. First, we prepared SiO_2/Si and GeO_2/Ge oxidized in $^{16}O_2$, then both were reoxidized in $^{18}O_2$. SIMS results clearly exhibit a significant difference of ^{18}O profile in the oxides. The result in SiO_2/Si system is as expected by the Deal-Grove type kinetics, while that in GeO_2/Ge shows rather flat profile of ^{18}O in GeO_2 and not ^{18}O accumulation at GeO_2/Ge interface. The results demonstrate a significant difference of oxidation kinetics between Si and Ge.

Results suggest that Ge oxidation should be described by kinetics completely different from the Deal-Grove model. Thus, we propose for the first time a new kinetic model of thermal oxidation of Ge, considering both O-vacancy and atomic O diffusion as a function of O_2 pressure. The model can reasonably explain anomalous O_2 pressure dependence in Ge oxidation as well. Furthermore, experimental results in the oxidation of SiO_2/GeO_2/Ge, GeO_2/SiO_2/Si and GeO_2/SiO_2/Ge stacks are also. They also strongly support the new kinetic model of Ge oxidation. This is critically important for achieving high quality Ge gate stacks, as the Deal-Grove model have played a significant role in Si technology.

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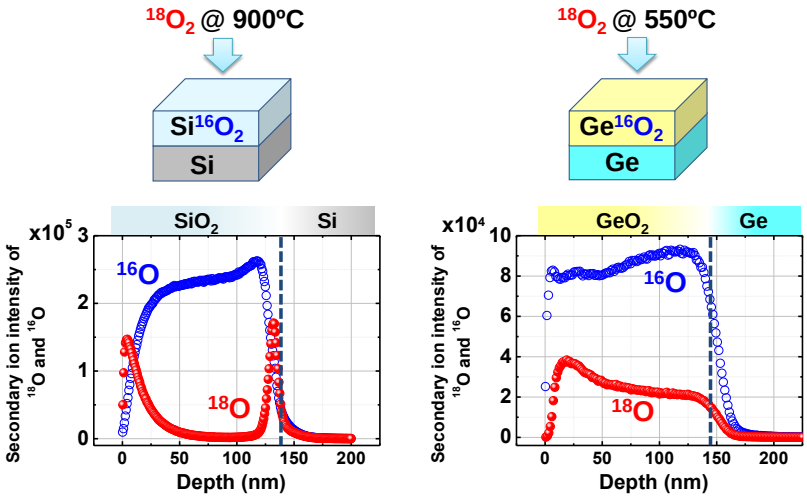

Figure 1 ^{18}O isotope tracing experiment in Si and Ge with SIMS. In Si, it is clearly reproduced that ^{18}O atoms are accumulated at the interface and that only a slight amount of ^{18}O exists in the film. While in Ge, ^{18}O has a rather flat profile inside GeO_2 film.

DEVELOPMENT OF HIGH PERFORMANCE METAL OXIDE THIN-FILM TRANSISTORS FOR OLED AND FLEXIBLE DISPLAY

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Key Words: IGZO, TFT, Metal Oxide Semiconductor, High Mobility.

ZnO based oxide semiconductors have attracted tremendous attention as a channel layer of pixel switching transistors in the LCD, OLED and flexible displays because they offer intriguing properties such as high mobility, extremely low leakage current and low cost fabrication cost compared to silicon based semiconductor. Since implementation of IGZO transistor into commercial high end LCD and large area OLED TV in 2012, the required carrier mobility of metal oxide thin-film transistors (TFTs) has been increasing rapidly to meet the demands of the ultra-high-resolution, large panel size and three dimensional visual effects as a megatrend of flat panel display.[1-2] However, the typical field-effect mobility of IGZO TFTs in the practical production line is less than 15 cm^2/Vs, which is still not enough to drive the high-end flat panel displays with $\geq$ 300 ppi, more than 60 inch and high frame rate ($\geq$ 240 Hz).[3] Approaches to improve the mobility of electron carriers in metal oxide TFT would involve the optimization of cation composition, stacked channel structure and the lattice ordering-induced crystallization.[4] In this presentation, we presented our recent efforts toward the high performance and good reliability, which included the double channel structure such as ZTO/IZO and ZTO/ITO, the metal-induced crystallization at a low temperature, and atomic layer deposited IGZO TFTs.

Acknowledgment
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INTRODUCTION ON ATOMIC LAYER DEPOSITION FOR HIGH-K DIELECTRIC & HIGH MOBILITY OXIDE SEMICONDUCTOR THIN FILM TRANSISTORS

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Key Words: Atomic Layer Deposition, Oxide Semiconductor, ITZO, ZrO_2, thin film transistor,

Amorphous oxide semiconductors have been widely studied for the potential use in flat panel displays such as active matrix liquid crystal display (LCD) and Organic light emitting diodes (OLEDs). Since reporting amorphous InGaZnO semiconductor thin film transistor (TFT) in 2003 & 2004, many multi-component oxide semiconductors have been intensively investigated and developed by reactive sputtering method. Very recently, the sputtered InGaZnO TFTs are already adopted in mass-production to fabricate AMOLED TVs. However, there remain several problems such as high mobility & stability issues. Also, virtual and argument reality (VR, AR) applications are rapidly emerging in display markets but the main issues are high resolution and low-voltage driving technologies.

Although there are considerable issues in oxide TFT applications, authors thought that high mobility oxide semiconductor and high-k gate insulator will be very important for the coming TFT devices. In this talk, those semiconductor and high-k dielectric will be discussed in terms of oxide TFT performances. All issued materials are deposited by plasma enhanced atomic layer deposition (PEALD), which is already adopted in Semiconductor industry. ALD is unique and reliable thin film deposition method below 50nm thickness due to very low process tact-time. In the first session, I will discuss ALD ITZO semiconductor thin film and the associated device performance. The ITZO ALD TFTs exhibited around 30cm^2/V.sec of mobility and low hysteresis (~0.2V). The content of SnO_2 is a very important key factor to control mobility and reliability. In second session, ALD deposited ZrO_2 thin film as a gate insulator will be discussed. The ZrO_2 thin film is getting crystallized as the deposition temperature increased from 200°C to 300°C. The crystallinity may help to increase dielectric constant but loose the mobility of oxide TFT due to the columbic effect. It will be discussed how to optimize ALD oxide semiconductor and dielectric materials to get best performance. Although ALD process is too early to use in Display Application, but ALD technique will be very useful for the coming challengeable device applications.

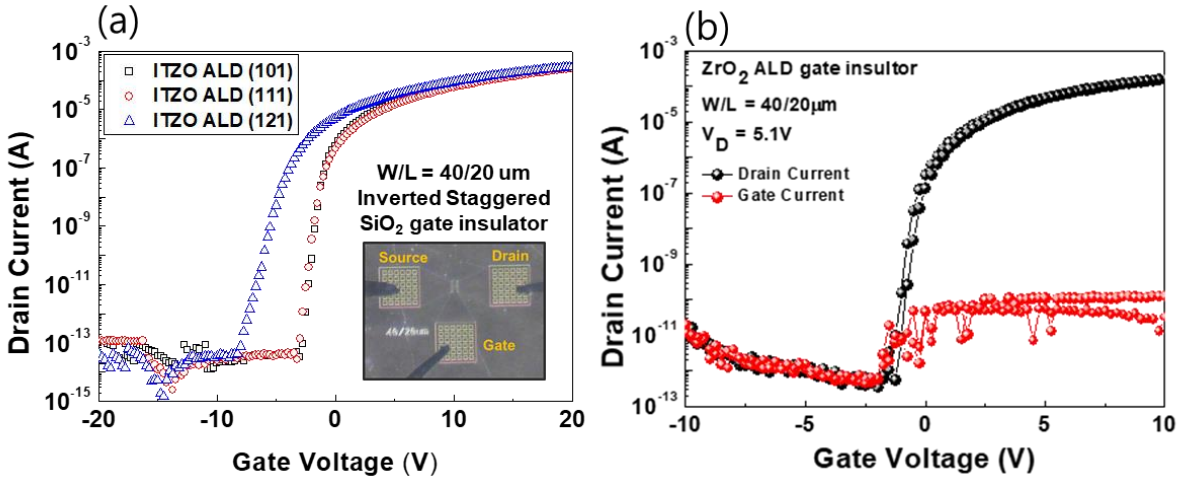

Figure 9 – (a) Representative Transfer curves of InSnZnO ALD oxide semiconductors with thermal SiO_2 gate insulators depending on ALD SnO_2 cycle. (b) Representative Transfer curve InSnZnO (sputtered) TFT with ALD ZrO2 gate insulators.

FLASH LAMP ANNEALED POLYCRYSTALLINE SILICON AS A POTENTIAL CANDIDATE FOR LARGE PANEL MANUFACTURING

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Key Words: TFT, LTPS, xenon flash-lamp, PMOS

The flat-panel display industry is in pursuit of TFT manufacturing processes which are cost-effective, easily scalable to large glass panels, and meet the performance requirements of advanced display products. While excimer laser anneal (ELA) low-temperature polycrystalline silicon (LTPS) can offer exceptional TFT performance, a lower grade LTPS may still satisfy product requirements at a lower production cost. Flash-Lamp Annealing (FLA) is an emerging candidate for the manufacture of LTPS. Multi-lamp exposure systems with high repetition pulse rates would potentially offer significant advantages in manufacturing throughput and cost over ELA. Techniques to overcome challenges that have hindered device scaling and reduction in variation of device operation are under investigation. The following presents a status update on the development of FLA Polycrystalline Silicon (FLAPS) technology.

The FLA equipment used for this work was a NovaCentrix PulseForge 3300 system, capable of uniform exposure of a 7 cm x 12 cm area at intensities as high as 50 kW/cm^2 over microseconds pulse duration. PMOS TFTs were fabricated using combinations of FLA, ion implantation and furnace annealing to define the source/drain and channel regions. Predefined polygons of 60 nm thick amorphous silicon vertically sandwiched between layers of SiO_2 were crystallized on Corning Lotus NXT display glass using single-pulse FLA exposure. The amorphous silicon melts while absorbing a sufficient fraction of the xenon emission spectrum, and becomes polycrystalline while staying within the thermal constraints of the underlying glass substrate. Boron dopant ions were implantation into the source/drain regions defined by lithographic patterning or a self-aligned gate strategy. Boron activation was realized by combinations of FLA, furnace annealing, and pre-amorphization using an electrically inactive species. FLA conditions following dopant introduction avoided silicon melting which causes significant lateral diffusion. Representative electrical characteristics are shown in figure 1. While the device operation demonstrates a general dependence on the degree of dopant activation, observations on the electrical characteristics indicate a complex relationship between defect states and the specific implant/activation strategy applied. The influence of doping strategy on both device performance and resistance to failure is the primary focus of this work. Additional experiments involving variations in the FLAPS morphology will also be discussed.

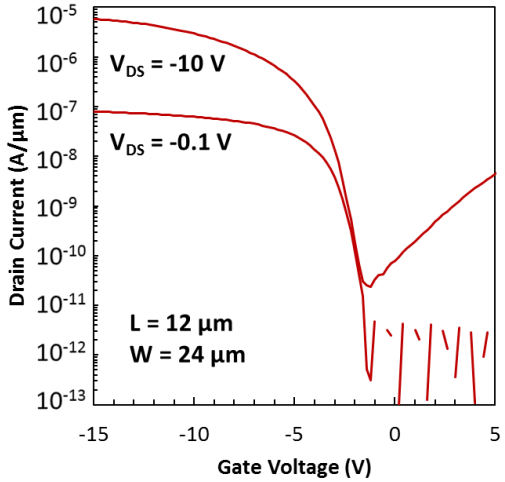

Figure 10 – I_D-V_{GS} Transfer Characteristics of FLAPS PMOS TFT which utilized $^{28}Si^+$ pre-amorphization prior to boron introduction and activation

HOMO-JUNCTION BOTTOM-GATE AMORPHOUS In–Ga–Zn–O TFTs WITH METAL INDUCED SOURCE /DRAIN REGIONS

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Key Words: Amorphous indium–gallium–zinc oxide, thin-film transistors, homo-junction, aluminum reaction.

A fabrication process for homo-junction bottom-gate (HJBG) amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) is proposed, in which the a-IGZO section as source/drain (S/D) region is induced to a low resistance state by coating a thin metal Al film and then performing a thermal annealing in oxygen, and that as channel region is protected from back etching by depositing and patterning a protective layer. Experimental results show that with a 5 nm Al film and a 200 ºC annealing, the sheet resistance of the S/D a-IGZO is 803 Ω/□ and keeps stable during subsequent thermal treatment. In addition, the annealing generated thin Al_2O_3 film contributes to improve the thermal stability and ambient atmosphere immunity of the fabricated HJBG TFTs.

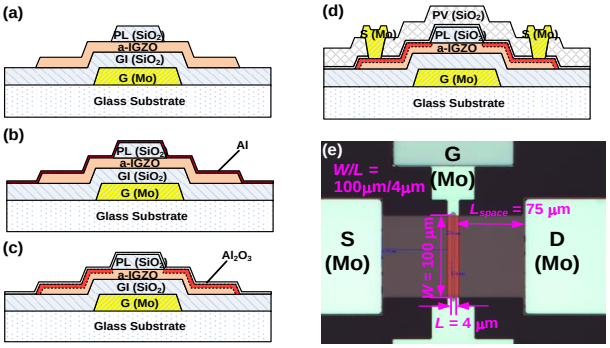

Fig. 1. Schematic fabrication steps of a-IGZO TFT

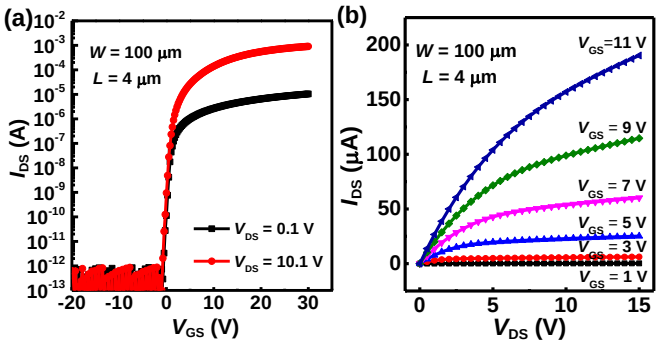

Fig. 2. Current–voltage (I – V) characteristics of a TFT in the proposed Al reacted HJBG process.

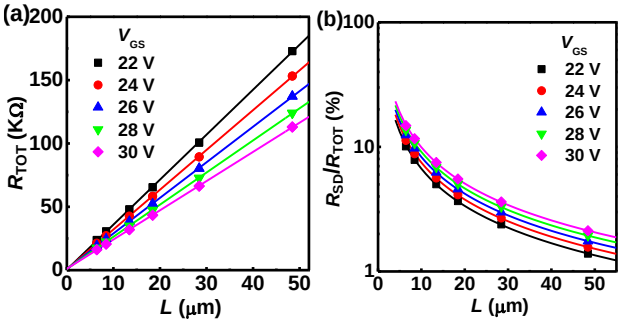

Fig. 3. (a) Total resistance and (b) ratio of source/drain parasitic resistance to the total resistance versus channel length.

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BACK-END OF LINE COMPATIBLE TRANSISTORS FOR HYBRID CMOS APPLICATIONS

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The low-temperature back-end of line (BEOL) compatible transparent amorphous oxide semiconductor (TAOS) TFTs and poly-Si TFTs are the suitable platforms for three-dimensional (3D) integration hybrid CMOS technologies. The n-channel amorphous indium tungsten oxide (a-IWO) ultra-thin-film transistors (UTFTs) have been successfully fabricated and demonstrated in the category of indium oxide based thin film transistors (TFTs). We have scaled down thickness of a-IWO channel to 4nm. The proposed a-IWO UTFTs with low operation voltages exhibit good electrical characteristics: near ideal subthreshold swing (S.S.) ~ 63mV/dec., high field-effect mobility (□FE) ~ 25.3 cm2/V-s. In addition, we also have fabricated the novel less metal contamination Ni-induced lateral crystallization (LC-NILC) p-channel poly-Si TFTs. The matched electrical characteristics of n-channel and p-channel devices with low operation voltage and low IOFF are exhibiting the promising candidate for future hybrid CMOS applications.

ADHESION LITHOGRAPHY FOR LARGE-AREA PATTERNING OF ASYMMETRIC NANOGAP ELECTRODES

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Key Words: Large-area fabrication, nanoscale devices, nanomanufacture.

As the resolution of devices in the electronics industry has hit the nanoscale, device fabrication costs have rapidly increased. Whilst commercial technologies such as electron-beam lithography are able to define nanoscale features, they are costly and unsuitable for large area electronics. Research is now focusing on fabrication techniques that can pattern features on the nanoscale on flexible substrates, over large areas without incurring these high costs, such as adhesion lithography (a-Lith). A-Lith is a large-scale fabrication technique for producing planar asymmetric nanogap electrodes [1]. Devices have been created with gap width:length aspect ratios >100000. The technique can be carried out in air and at ambient temperature making it ideal for the field of plastic electronics [2].

The a-Lith technique relies on a self-assembled monolayer (SAM) molecule selectively coating a prepatterned metal (M1) which then changes the adhesion forces. A second metal (M2) is then deposited over the top and can be specifically patterned when peeled using an adhesive due to its reduced adhesion on M1 relative to elsewhere. M2 only remains in the areas where there is no M1 (in the areas where it directly contacts the substrate). Where M2 fractures at the edge of M1, a nanogap (≈10 nm) is formed between the two metals [1].

A-Lith has shown improved device performance across many areas of device electronics as the ability to pattern electrodes side-by-side largely eliminates parasitic capacitances. Such electrodes have been utilized in device applications including high responsivity photodiodes [3], nano organic light emitting diodes [4], memristors [2] and high speed diodes [5]. This fabrication technique was previously only successfully carried out with Al, Au and Ti as M1, and Al and Au as M2, with the Al and Au (with an Al adhesion layer) thermally evaporated. In this work, a-Lith has been successful executed with a variety of materials sputtered including Cu, Ni, Ti, Mo, Cr and Al as M1. M2 is shown to be successful with Al, Ni, Cu and Cr. This has allowed for further devices applications to be explored including devices utilizing 2D materials.

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DIRECTED SELF-ASSEMBLY OF BLOCK COPOLYMERS FOR SUB-10NM FABRICATION

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Directed self-assembly of block copolymers, based on microphase separation, is a promising strategy for high-volume and cost-effective nanofabrication. Over the past decades, manufacturing techniques have been made huge progress that it is now possible to engineer complex systems of heterogeneous materials around a few tens of nanometers (Such as 193i lithography). Further evolution of these techniques, however, is faced with difficult challenges not only because of diffraction limit, but also in prohibitively high capital equipment costs. Materials that self-assemble, on the other hand, spontaneously form nanostructures down to length scales at the molecular scale, but the micrometer areas or volumes over which the materials self-assemble with adequate perfection in structure is incommensurate with the macroscopic dimensions of devices and systems of devices of industrial relevance. Directed Self-Assembly (DSA) refers to the integration of self-assembling materials with traditional manufacturing processes. The key concept of DSA is to take advantage of the self-assembling properties of materials and at the same time meet the constraints of manufacturing. Technically DSA is similar to the double patterning in terms of resolution enhancement. In this report we will discuss the use of lithographically-defined chemically patterned surfaces to direct the assembly of block copolymer films for semiconductor manufacturing.

NEUROMORPHIC SYSTEM USING THIN-FILM DEVICES

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Key Words: Neuromorphic system, Thin-film device, Amorphous metal-oxide semiconductor (AOS).

Artificial intelligences are essential concepts in smart societies, and neural networks are typical schemes that imitate human brains. However, conventionally, neural networks are realized using complicated software and high-spec hardware, whose machine size is large and power consumption is also huge. On the other hand, neuromorphic systems are composed only of customized hardware, whose machine size can be small and power consumption can be reduced.
In this study, neuromorphic systems using thin-film devices, especially with amorphous metal-oxide semiconductor (AOS), have been developed[1]. Here, analog memory, which is utilized as synaptic weight, is proposed. The electrical conductance of the AOS devices is employed as the analogy memory. Moreover, modified Hebbian learning, which is local learning rule without extra control circuits, is proposed. The conductance deterioration of the AOS devices is employed as synaptic plasticity.
First, a Hopfield neural network with AOS devices as crosspoint-type synapse elements has been actually fabricated to confirm the fundamental operation of the neuromorphic system using thin-film devices. It is found that the electric current continuously decreases along the bias time. The Hopfield neural network is really assembled using a field-programmable gate array (FPGA) chip and connecting the AOS devices to the FPGA chip. It is confirmed that a necessary function of the letter recognition is obtained after learning process.
Next, a cellular neural network with AOS devices as layered-type synapse elements has been also actually fabricated. It is again found that the electric current continuously decreases along the bias time. The cellular neural network is also really assembled using a large-scale integration (LSI) chip and depositing the AOS devices on the LSI chip. It is also confirmed that a necessary function of the letter recognition is obtained after learning process.
Once the fundamental operations are confirmed, more advanced functions will be obtained by scaling up the devices and circuits. Therefore, it is expected the neuromorphic systems can be three-dimensional (3D) integration chip, the machine size can be compact, power consumption can be low, and various functions of human brains will be obtained. What has been developed in this study will be the sole solution to realize them.

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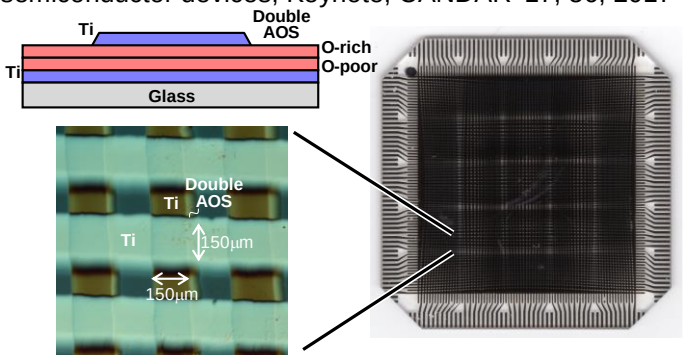
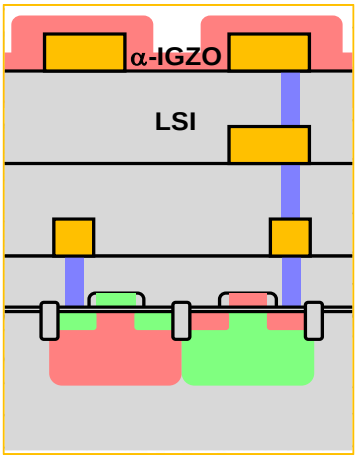


Figure 1 – AOS devices as crosspoint-type synapse elements



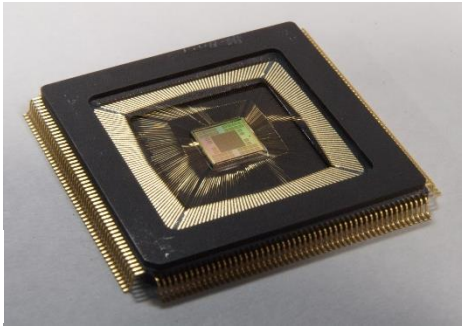


Figure 2 – Neuromorphic system using an LSI chip and AOS devices deposited on it

STATEFUL IN-MEMORY COMPUTING IN EMERGING CROSSBAR MEMORIES

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Key Words: In-memory computing, emerging semiconductor technology, Memristor

Emerging memories such as MRAM, PRAM, and RRAM have been extensively studied due to its various advantages over the conventional memories. Because their performances are yet better than the conventional memories as DRAM and NAND Flash, researchers are primarily trying to find their applications at embedded memory or storages class memory applications. As such, when the emerging memories are used for memory or data storage, its application can be very limited to one of the computing elements in the conventional computing hierarchy. If an entirely new function—a computing function—can be implemented in the emerging memories, it could destroy the traditional computing hierarchy and change the computing paradigm. The stateful in-memory computing technology provides such capability to the emerging memories. The first concept of stateful logic was proposed in 2010 by the group of HP using the crossbar RRAM. Afterward, there have been many advancements for putting the technology into practical use. In this presentation, the most up-to-date stateful in-memory computing technology is presented. The stateful in-memory computing technology can apply to any emerging memories based on the crossbar architecture. Therefore, it would be an additional beneficial option for the emerging memories strengthening its functionality more than memory or storage.

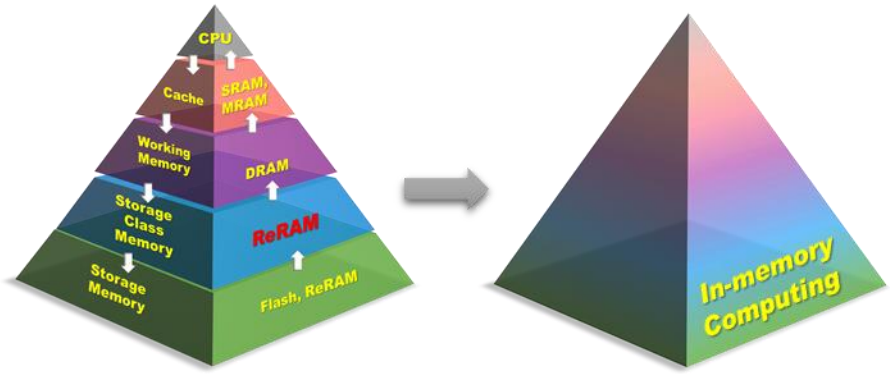

Figure 11 – A conceptual schematic showing the computing hierarchy change by the in-memory computing technology

MEMRISTIVE CROSSBAR ARRAYS FOR BRAIN-INSPIRED COMPUTING

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Key Words: resistance switch; memristive device; analog computing; neuromorphic computing

While the speed-energy efficiency of traditional digital processors approach a plateau because of limitations in transistor scaling and the von Neumann architecture, computing systems augmented with emerging devices such as memristors offer an attractive solution. A memristor, also known as a resistance switch, is an electronic device whose internal resistance state is dependent on the history of the current and/or voltage it has experienced. With their working mechanisms based on ion migration, the switching dynamics and electrical behavior of memristors closely resemble those of biological synapses and neurons. Because of its small size and fast switching speed, a memristor consumes a small amount of energy to update the internal state (training). Built into large-scale crossbar arrays, memristors perform in-memory computing by utilizing physical laws, such as Ohm's law for multiplication and Kirchhoff's current law for accumulation. The current readout at all columns (inference) is finished simultaneously regardless of the array size, offering a huge parallelism and hence superior computing throughput. The ability to directly interface with analog signals from sensors, without analog/digital conversion, could further reduce the processing time and energy overhead.

We developed memristive devices based on foundry compatible materials such as silicon oxide and halfnium oxide [1,2]. We demonstrated two nanometer scalability [3] and eight layer stackbility [4] with these devices. Furthermore, we integrated the halfnium oxide memristors into large analog crossbar arrays for analog signal and image processing [5], and the implemented multilayer memristor neural networks for machine learning applications [6,7]. The crossbar arrays were also used for other applications such as hardware security [8].

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EMERGING APPLICATIONS OF TFTS ENABLED BY NOVEL DEVICE ARCHITECTURES

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Key Words: TFT, Dual Gate, Field Coupling, Emerging Applications

Being a fundamental technology that drives large-area electronics such as flat panel displays, thin-film transistor (TFT) technology has experienced a rapid growth over the last decade due to a vast adoption of consumer electronics such as smart phones and TVs. In the display either AMLCDs or AMOLEDs, a TFT acts as a switch or forms a pixel driving circuit. It is an electronically-active device without sensing/transducing functionality or intelligence. Architecture wise, it often consists of three terminals of gate, source and drain like a MOSFET.

Recently, the potential of TFTs in non-display applications has been take a serious revisit mainly due to emerging new markets such as IOTs, wearable electronics and human-machine interface. These non-display applications can become new driven force for large-area electronics in the coming era. In order to enable such applications, the TFT requires a design change especially in the architectural level. We hereby propose a dual-gate field-coupled TFT architecture where its top gate is field-sensitive and its bottom gate is for control. The optical, mechanical, and thermal fields can be coupled and the output of the dual-gate TFT depends on strength of the external stimuli. In this talk, I will address some emerging applications including optical sensing and imaging, tactile sensing and electronic skin, wearable health monitoring, energy harvesting and etc. Conventional material systems forming the TFTs including amorphous silicon, low temperature polysilicon, and oxide semiconductors will be discussed.

NANO-RESISTORS BASED DEVICES – EFFECTS OF SIZE AND STRUCTURE ON PERFORMANCE

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Key Words: nano-resistors, MOS, high-k, SSI-LEDs, memories

Recently, a new type of nano-resistor device that can emit the broad bad ward white light as well as show the diode-like behavior has been reported (1,2,3). They are potentially applicable to lighting, on-chip interconnects, nonvolatile memories, nano-heaters, etc. The nan-resistor device can be operated continuously for more than 20,000 hours in air without a passivation layer. The unique phenomenon of simultaneously formation of a large number of nm-sized nano-resistors from the breakdown of a MOS capacitor was never reported in the open literature until our publication.

In this paper, new results on nano-resistor devices will be discussed. The device size effect on the light emission phenomenon, as shown in Fig. 1, will be explained from the distribution of nano-resistors across the gate electrode and the nano-resistor formation mechanism. In addition, the increase of the light emission efficiency from the embedding of nanocrystals in the gate dielectric layer will be discussed based on defects enhanced nano-resistors formation process. Furthermore, for the large array application, the crosstalk among adjacent devices can be avoided using the coplanar structure, which will be shown in this paper. The device performance will be compared with that of the vertical-structured device.

In summary, nano-resistor devices are easily fabricated with IC compatible materials and processes. They are medium power devices complimentary to IC as well as other electronics and optoelectronics.

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Figure 1. Nano-resistor devices of different diameters.

PERFORMANCE ENHANCEMENT Of SSI-LEDs AND GEOMETRICALLY CONFINEMENT OF LIGHTING DOTS BY USING PATTERNED WAFER APPROACHES

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Key Words: HfO_2, patterned wafer, light emission device.

Solid state incandescent light emitting devices (SSI-LEDs) were first demonstrated in 2013 by Kuo's group, which have the metal-oxide-semiconductor structure and emit white light directly[1]. The conductive filaments (CFs) through CAFM figures out that Si wafer has a significant impact on the device performance[2, 3], multiplayer dielectric layers structure have also been study to enhance the light emission[4]. We demonstrate two approaches to improve the performance of SSI-LEDs by using patterned wafer in this work.

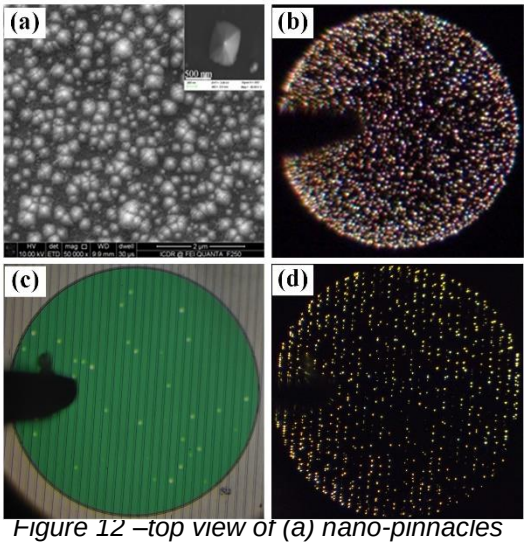

Figure 12 –top view of (a) nano-pinnacles and (b) nano-stripes; lighting photos of devices with (c) nano-pinnacles and (d) nano-stripes

One way employs the auxiliary structure of nano-pinnacles on Si wafer to prepare SSI-LEDs consisting of HfO_x-ZnO-HfO_x/In_2O_3-SnO_2 (ITO). Fig. 1(a) is the top view SEM image of the nano-pinnacle of Si wafer, which shows lots of nano pyramids on the surface. Fig. 1(b) represents the lighting photo from device with nano-pinnacle. When ~230×140 nm pyramids are prepared onto silicon wafer by wet-etching, the electric field strength is enhanced due to the nano-pinnacles, inducing the connection of the defects in the dielectric stack and forming more continuous conductive paths. The onset voltage of light emission is decreased by 60%, and almost one order of emission intensity is improved with the structure of nano-pinnacles.

The other way employs the regular nano-stripe Si wafer to prepare SSI-LEDs consisting of Ti-HfO_2/In_2O_3-SnO_2 (ITO).The height and width of nano-stripe are 100 nm and 3 μm, respectively. The wafer is covered by the stack layer mentioned above. Fig. 1(c) is the top view of the device with regular nano black lines arrayed. Fig. 1(d) is the lighting photo from the device with patterned nano-stripe. From Fig. 1 (d), an obvious regular distribution of lighting dot can be observed which demonstrates that the regular distribution is related to the geometrical confinement of electric field at the edge of the nano-stripe. The enhanced electric field can make it easier for the hard breakdown of HfO_2 thus more CFs would prefer to be generated. Furthermore, the density of the lighting dots is increased by the patterned wafer. The number of the lighting dots for the device with patterned wafer is increased to $1.02 \times 10^7/cm^2$ compared with $1.56 \times 10^6/cm^2$ for the device with normal planar wafer. The light emission is also brighter due to the increase of lighting dot.

In summary, the nano-structure on wafer helps to increase of the lighting dots of SSI-LEDs. The distribution of lighting dots is confined by the patterned wafer. This attributes not only to the performance improvement of SSI-LEDs but also to the position of lighting dot during the micro-measurement process. The proposed approach shows great value to improve the optical performance of SSI-LEDs.

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MICROSYSTEMS FOR THERMAL ENERGY POWERING

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Key Words: Thermoelectric power generation, Electrodeposition, Microfabrication, Energy harvester, Super capacitor

Flexible thermoelectric micro power generators have been developed for wearable devices such as body area network. Also in order to store the generated power, a micro solid state supercapacitor using thin films composed of graphene nanowall are developed. The flexible thermoelectric micro power generator is fabricated by electrochemical deposition of Bi_2Te_3 and Sb_2Te_3, which is embedded by PDMS, as shown in Fig. 1. A power generation of 4 $\mu W/cm^2$ are demonstrated from human body temperature. In order to improve the power generation performance, nanocomposites of Bi_2Te_3 and Au nanoparticles are synthesized by co-electrodeposition (Fig. 2). For the fabrication of the solid state micro super capacitor, plasma-enhanced chemical vapor deposition is used to deposit graphene nanowall on a spiral-shaped silicon electrode pattern (Fig. 3). On the graphene nanowall Ru oxide or Ni oxide is deposited for charge storage layer. Areal energy density of ~15 $\mu Wh/cm^2$ and areal power density of ~2.49 mW/cm^2 are achieved. Also a wide operation voltage range will allow to the application to energy storage of the thermoelectric power generator.

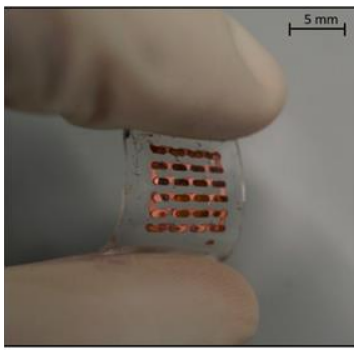

Figure 1. Developed Flexible power generator based on electroplated Bi_2Te_3-Sb_2Te_3.

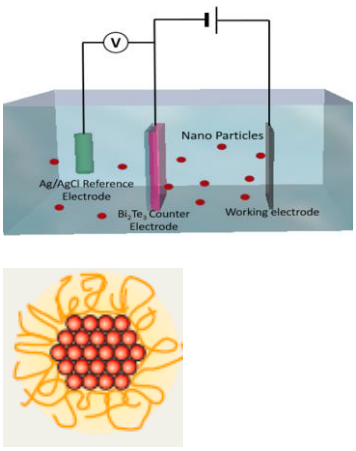

Figure 2. Metal Nanoparticle inclusion method using co-electrodeposition.

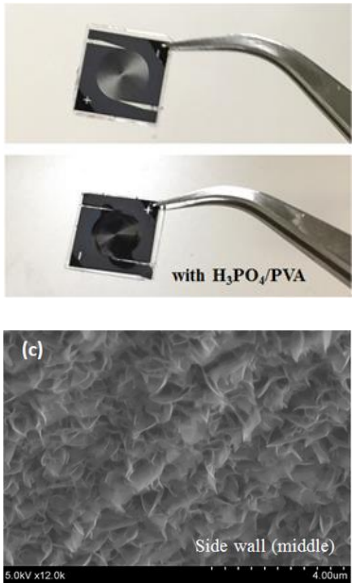

Figure 3. Carbon nanowall based solid state micro-supercapacitor

CHEMIRESISTIVE AND RESISTIVE SWITCHING SEMICONDUCTOR BASED SENSOR FOR BIOMOLECULE DETECTION

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Key Words; Resistive switching, Chemiresistor, Graphene, Biosensor, Cortisol.

Recently, chemiresistive semiconductor, which varies its resistance or conductance status based on chemical phenomena at its surface, has been developed as a sensor device for biomolecule detection. Particularly, graphene has been one of the best example for the chemiresistive semiconductors, even for resistive switching semiconductors. In addition, the graphene is two-dimensional (2D) carbon structure having a large surface area, where significant biosensing applications have been continuously reported. In this study, we demonstrated reduced graphene oxide (rGO) biosensor structure for a stress hormone, i.e. cortisol, sensing. The device structure was stepwise self-assembly monolayers (SAMs) stacked by reduced graphene oxide between source and drain. Then, cortisol monoclonal antibody (c-Mab) was chemically tethered on reduced graphene oxide layer for the cortisol detection by its specific antigen-antibody binding. The current versus voltage (I-V) curve exhibited resistance changes and resistive switching I-V behaviors as a sensing mechanism, which demonstrated a unique possibility of rGO semiconductor based sensor. Also, chemiresistance change in the forms of resistance ratio was calibrated in terms of sensing cortisol concentration as shown in Figure 1.

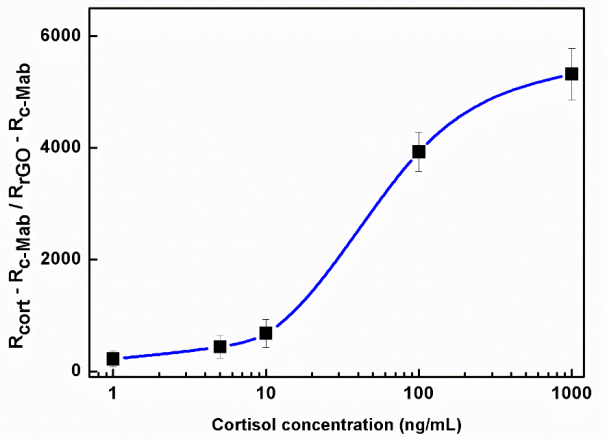

Figure 13 – Chemiresistance calibration plot of various concentration of cortisol solution on the 53 nm thick sensor